NAVAL POSTGRADUATE SCHOOL
MONTEREY, CALIFORNIA

THESIS

SWITCH POWER AMPLIFIER FOR TAR3

by

Eric Wesley Moore

June 1995

Thesis Advisor: Thomas J. Hofler
Thesis Co-Advisor: Sherif Michael

Approved for public release; distribution is unlimited

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	June 1995	Master's Thesis

4. TITLE AND SUBTITLE
Switching Power Amplifier for TAR3

5. FUNDING NUMBERS

6. AUTHOR(S)
Moore, Eric W.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Naval Postgraduate School
Monterey, CA 93943-5000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the United States Government.

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

This thesis describes the theory, design, construction, and testing of a switching power amplifier. The major emphasis of the research and development effort reported herein is to design and construct an efficient power amplifier for varying load conditions which provides 40 Watts of power, at 85% efficiency, and with no more than 10% harmonic distortion. The power amplifier will need one voltage supply and one input audio signal. The amplifier will be used to power demonstration thermoacoustic refrigerators and the Hofler third generation thermoacoustic refrigerator, TAR3.

14. SUBJECT TERMS	15. NUMBER OF PAGES
switching power amplifier, thermoacoustic refrigerator, CMOS amplifier	80
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. Z39-18
298-102

Approved for public release; distribution is unlimited.

SWITCHING POWER AMPLIFIER FOR TAR3

Eric Wesley Moore
Naval Postgraduate School B.S. (1992)

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
June 1995

Author: Eric Wesley Moore
Eric Wesley Moore

Approved by: Thomas J. Hofler, Thesis Co-Advisor

Sherif Michael, Thesis Co-Advisor

Michael A. Morgan, Chairman,
Department of Electrical and Computer Engineering

ABSTRACT

This thesis describes the theory, design, construction, and testing of a switching power amplifier. The major emphasis of the research and development effort reported herein is to design and construct an efficient power amplifier for varying load conditions which provides 40 Watts of power, at 85% efficiency, and with no more than 10% harmonic distortion. The power amplifier will need one voltage supply and one input audio signal. The amplifier will be used to power demonstration thermoacoustic refrigerators and the Hofler third generation thermoacoustic refrigerator, TAR3.

TABLE OF CONTENTS

I. INTRODUCTION

The power amplifier described herein is to be a new subsystem to the third generation thermoacoustic refrigerator by Hofler. The amplifier is required to provide 40 Watts of power with 80% efficiency and 10% distortion. The design of the switching power amplifier for this thesis was adapted from a design by L. Decker of Cinncinati, Ohio[Ref. 1]. The design was modified for use with the third generation thermoacoustic refrigerator. The introductory material includes some theory of switching power devices and thermoacoustics that is applicable and relevant to this experiment. The theory of switching power amplifiers and filters are also covered in more detail.

A. BRIEF HISTORY OF TAR3

Thermoacoustics can be defined as the conversion of energy from one form to another by use of sound propagation and heat flow. The study of thermoacoustics goes back to the late 18th century, but it was not until Rott's work[Ref. 2] in the late 1970's and early 1980's were there any major breakthroughs in the field. Hofler was able to numerically solve Rott's equations and build a working thermoacoustic refrigerator at Los Alamos National Laboratory as he pursued his Doctoral degree [Ref. 3]. TAR3 is Hofler's third generation thermoacoustic refrigerator.

This heat pump system, which comprises the working part of the refrigerator, consists of a pressurized 1/4 wavelength resonator tube driven at one end by an electrodynamic loudspeaker operating at approximately 500Hz.

The eletrical driver impedance of the loudspeaker is the most important variable in the design of the switching power amplifier. This thesis will be restricted to this factor for design purposes.

B. THEORY OF SWITCHING POWER DEVICES

High frequency switching techniques are used almost exclusively in today's electronic equipment. High frequency pulse-modulated waveforms can be used to switch power transistors on and off. The use of power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), rather than power bipolar transistors, allows switching frequencies as high as 100kHz to be used. The theory of a switching transistor is that it has two states:

ON: all current and no voltage across the device.

OFF: no current and all voltage across the device.

In an ideal situation, the transistor acts as a switch allowing either maximum current to flow or no current to flow. The theoretical power dissipated in such a device is given by

$$P = VI = 0. \tag{1.1}$$

All of the power is delivered to the load.

However, this is not the case with real electronic components. In reality, the power devices used typically have a small but significant resistance when the device is on and a very small leakage current when the device is off.

Furthermore, the brief time that a device spends between the on and off states may cause significant power loss. The power MOSFET devices used in the switching power amplifier for this research will dissipate only a small percentage of the total power delivered to the load.

II. CIRCUIT DESCRIPTION

The circuit chosen for the switching power amplifier is a prize winning design by Larry Decker of Cincinnati, Ohio [Ref. 1]. The schematic of the circuit is shown in Figure 2.1.

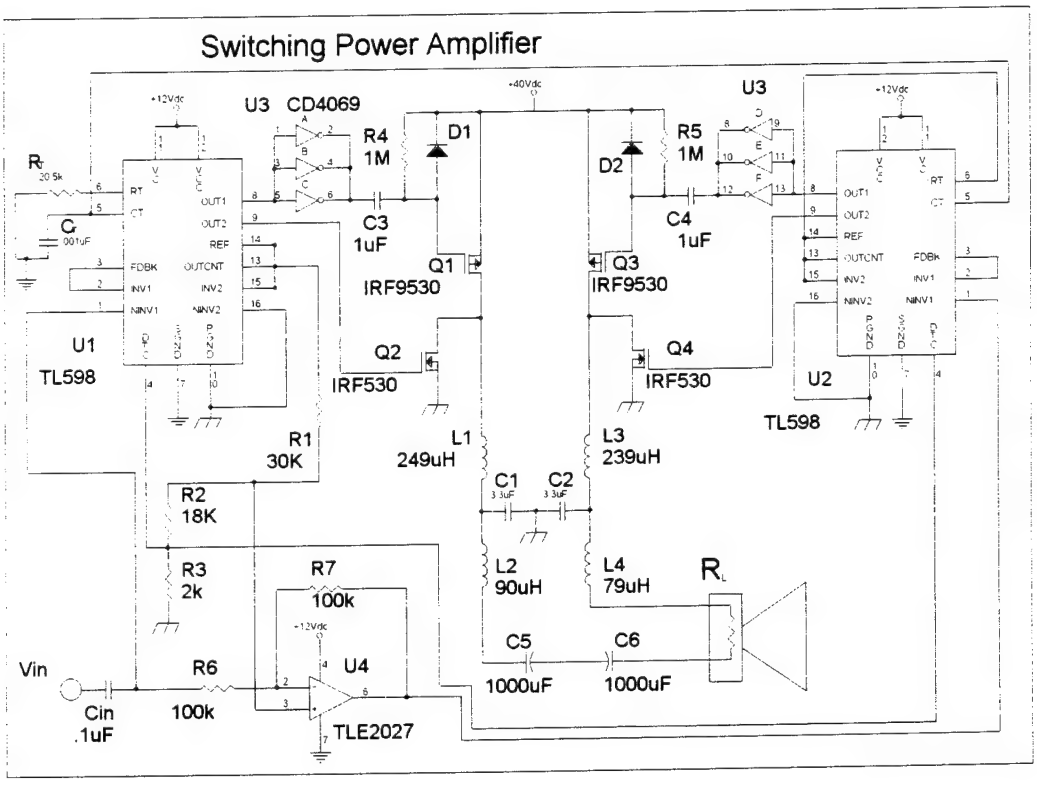

Figure 2.1 Switching Power Amplifier

The core of this switching power amplifier design is a TL598 pulse-width-modulation chip. The design utilizes two of these chips in a bridged (push-pull)

amplifier configuration. Resistor R_T and capacitor C_T externally control the oscillator frequency of both pulse-width-modulation chips. A carrier frequency of 50kHz was chosen to simplify circuit design. The carrier frequency is a square wave signal, whose duty cycle is modulated by the user's audio input signal. The output of the TL598 turns the Field Effect Transistors (FETs) Q1 and Q2 on and off quickly. The output of the FETs are then filtered by two 3-pole low-pass Butterworth filters to remove the 50kHz carrier frequency. An operational amplifier is used to invert the user's audio input modulating signal which is then connected to the non-inverting input of the second TL598 pulse-width-modulation chip. The second TL598 chip's internal frequency is controlled by slaving it to the first TL598 chip. The second TL598 chip turns on and off FETs Q3 and Q4. The outputs of Q3 and Q4 are then fed to the second 3-pole Butterworth filter to remove the 50kHz carrier frequency. The outputs of the filters are then attached to the loudspeaker.

A. PULSE-WIDTH-MODULATION CHIP

Texas Instruments manufactures a number of pulse-width-modulation control circuits, including MC34060, SG2524, SG3524, TL493, TL494, TL495, TL594, TL595, and the TL598 which the Decker circuit utilizes. These chips vary from a single input error voltage amplifier and a single output transistor to dual error voltage or error current amplifiers and dual output transistors. The prevalent characteristics of these chips are an externally controlled oscillator frequency limited to 300kHz , output transistors capable of sourcing or sinking 200mA of current, 40Vdc maximum supply voltage, and an internal precision

voltage reference of 5Vdc. The specification sheets for these chips can be found in Ref. [5].

The TL598 pulse-width-modulation chip is typically used to construct controlled pulse-width-modulation circuits for power supplies. It incorporates all the necessary functions needed to build the switching power amplifier.

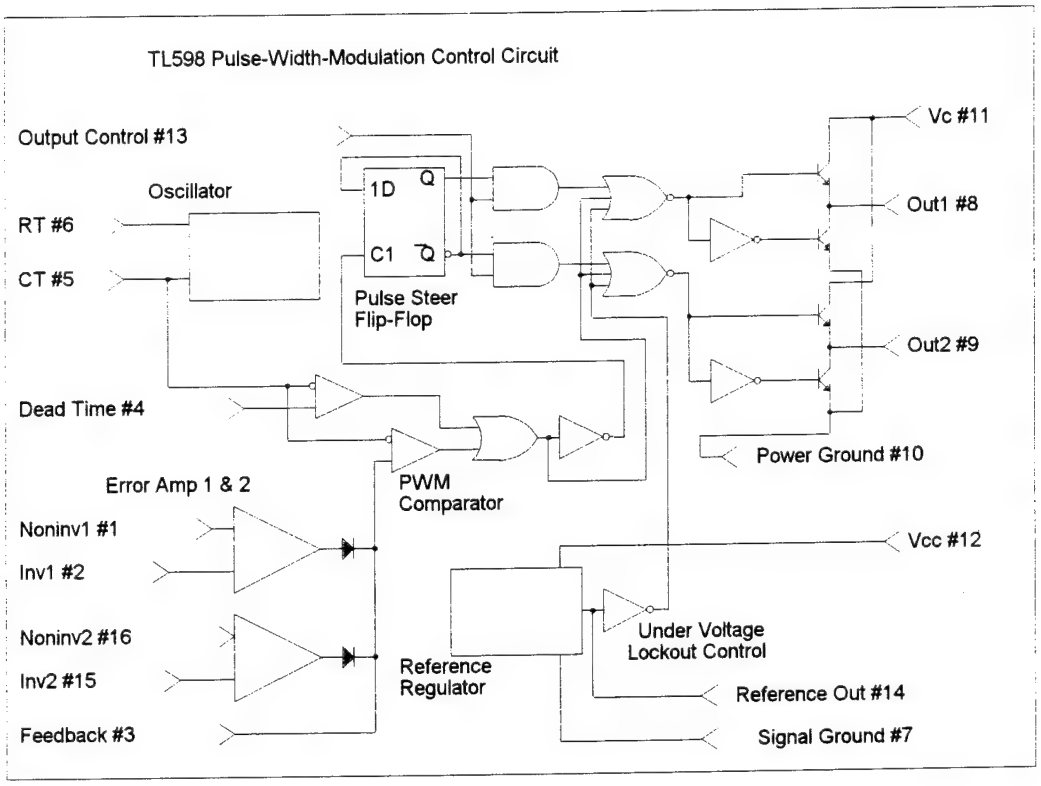

Figure 2.2 TL598 Pulse-Width-Modulation Control Circuit

The switching power amplifier could be constructed of discrete components, but the chip count would increase. A schematic of the inner circuitry of the TL598 chip is shown in Figure 2.2.

The TL598 contains an internal oscillator, two error amplifiers, separate power and signal grounds, a dead-time control circuit, a feedback network, a 5 V_{DC} precision reference, two totem-pole outputs, a pulse steering flip-flop, and an under-voltage lockout circuit.

The oscillator frequency in this configuration is set by R_T = 20.5 kΩ and C_T = .001 μF for 50kHz operation. The data sheet for the TL598 provides a graph of oscillator frequency and frequency variation versus timing resistance for selecting the values for timing resistor R_T and timing capacitor C_T. The oscillator output can be measured at pin #5 of the TL598. This is a sawtooth waveform from 0 to 3 V.

Frequency measurements were taken to verify the manufacturer's data. The initial resistance value for timing resistor, R_T, was chosen as 3.09 kΩ and the initial value for the timing capacitor, C_T, was chosen as .01 μF. The oscillator frequency measurements were taken with a frequency counter. The initial configuration resulted in an oscillator frequency of 38.6 kHz. The values for R_T and C_T were then varied until an oscillator frequency of 50kHz ± 1% was observed. Table 2.1 shows five combinations of timing resistors and timing capacitors that were used in the design before finding the final values for R_T and C_T. It was found that the graph in the data sheet for the TL598 was not entirely correct.

The oscillator signal is compared with the dead-time voltage input and the error amplifier input. The function of the dead-time comparator is to ensure that the two output transistors, pins #8 and #9, are never to conduct at the same time. If the dead-time control section pin is grounded, there is an internal voltage reference of .1V_{DC} on pin #4 to guarantee at least a 5% dead-time. The

oscillator is also compared to the input audio signal, pin #1, at the pulse-width modulation comparator. The input signal, after being half-wave rectified by the diode on the output of the error amplifier, is fed to the non-inverting input of the pulse-width-modulation comparator. The oscillator signal is fed to the inverting input of the comparator and compared with the input signal. The comparator produces a high, when the input signal exceeds that of the oscillator signal, and a low when the oscillator signal exceeds that of the input signal. The output of

Resistance R_T (Ω)	Capacitance C_T (μF)	Oscillator Frequency (Hz)	Sawtooth Amplitude(Vpk)
3090	.01	38600	3
27400	.001	40400	3
24300	.001	45300	3
19900	.001	54500	3
20500	.001	51600	3

Table 2.1 Resistance And Capacitance vs. Frequency

the pulse-width-modulation comparator is then fed to one of two inputs of an OR gate. The other OR gate input is the output of the dead-time comparator. If either or both of these two inputs is high, the output of the OR gate is high. The output of the OR gate is connected to three circuit components. It feeds an input of both three-input NOR gates located in the output section and feeds an inverter which is then connected to the clocking input of the pulse-steering flip-flop. The 1D input of the flip-flop is attached to the QNOT output of the flip-flop. The

two outputs, Q and QNOT, of the flip-flop are complimentary outputs. That is, when one is high the other is low. These two outputs are then connected to the two AND gates in the output section. The AND gates are only necessary in the push-pull configuration. The output control, pin #13, also feeds the two AND gates. If the output control is tied to ground, these AND gates would have no effect on the operation of the output transistors since the TL598 chip is in the parallel mode of operation. During parallel operation of the TL598 circuit, the output of the AND gates always assumes low state. However, if the output control pin is tied high, $5V_{DC}$, the AND gates would assume high and low states as the flip-flop changes state. The outputs from the AND gates then pass through the output 3-input NOR gate to switch the Output NPN transistors on and off quickly. The voltage Vc for output transistor operation is pin #11 and the power ground for the transistors is pin #10. The transistor outputs are capable of sourcing or sinking 200mA of current.

B. THE DECKER CIRCUIT

Decker's circuit, Figure 2.1, was built and tested. The theoretical operation of the circuit can be broken down into three sections:

1. Pulse-Width-Modulation
2. Power Field Effect Transistors (FETs)
3. Output Filtering

1. Pulse-Width-Modulation

The TL598 chip was employed to pulse-width-modulate a 50kHz carrier with a 500Hz audio signal. The input audio signal is capacitively coupled

through C_{in} to the non-inverting input of the first error amplifier of the TL598 chip. The inverting input of the error amplifier is connected to the feedback pin #3 of the TL598 chip. The second error amplifier is disabled by connecting the $5V_{DC}$ reference to the inverting input, pin #15, and grounding the non-inverting input, pin #16. The timing resistor R_T and timing capacitor C_T are connected to pins #6 and #5 respectively. This configuration sets the switching frequency. The $5V_{DC}$ reference, pin #14, is connected to the output control pin #13 for push-pull operation. The $5V_{DC}$ reference is also connected to the second error amplifier inverting input, as mentioned above, and to a resistor network made up of R1, R2, and R3. The resistor network produces two other voltage values used by other parts of the circuit. One of the voltages is $1V_{DC}$ that is used to bias the non-inverting input of operational amplifier U4. This voltage limits the input voltage of the input audio signal to 1Vpp maximum. The operational amplifier is used to invert the input signal for the second TL598 chip. The operational amplifier is set for a unity gain by resistors R6 and R7. The formula for calculating gain and phase for this operational amplifier is given by

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R7}{R6} = -\frac{100\,k}{100\,k} = -1. \qquad (2.1)$$

The inverted output of U4 is then connected to the second TL598's non-inverting input of the first error amplifier, pin#1. The second part of the resistor network provides .2 V_{DC} to set the dead-time control at pin #4 of both U1 and U2. This ensures no overlap occurs at the output transistors.

2. Power Metal-Oxide Semiconductor Field Effect Transistors (MOSFETs)

Two different Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) were utilized in the original Decker circuit. The 9530, a p-channel device, and the 530, an n-channel device, were found to have a low on-state impedance and high off-state impedance needed for this switching power amplifier. The transistors are labeled Q1, Q2, Q3, and Q4 in Figure 2.1.

The gates of the n-channel devices Q2 and Q4 are directly connected to pin #9 of the output transistors of U1 and U2 amplifiers. The gate lead of the p-channel 9530 , Q1, is the leftmost pin of the T0-220 package. The drain pin is the center pin of the package and the source pin is the rightmost pin of the package. The source of the n-channel 530 is connected to power ground. The drain of the n-channel 530, Q2, is connected to the input of the filter made up of inductor L1, capacitor C1, inductor L2, and the drain of p-channel device Q1.

The operation of Q2 depends on the gate-to-source voltage, Vgs. If the gate-to-source voltage exceeds +4 volts the power MOSFET allows some current to flow. The higher the gate-to-source voltage the lower the drain to source resistance until the transistor saturates. The MOSFET saturates at a Vgs $\approx$ 8 V_{DC}. It behaves more efficiently in the saturation region. The n-channel 530 has a maximum drain to source voltage, Vds, of 100V_{DC}. The static drain-to-source on-state resistance is typically .14 Ohms.

The gates of the 9530 p-channel devices are connected to pin #8 of U1 and U2 chips. However, there is some intermediate circuitry in this connection. The output transistor pin #8 of U1 is inverted using a CMOS 4000 series chip, U3. The output from pin #8 is a square wave of amplitude 0 to 12V_{DC}. A CMOS chip

4069 Hex Inverter, U3, is utilized to invert this waveform. Three inverters are used in parallel for each pin #8 of the TL598 chips U1 and U2. A CMOS 4000 series inverter chip is necessary because the voltage supply for the TL598 is 12V and a typical TTL chip can only handle $5V_{DC}$. The inverted modulated waveform from U1 is capacitively coupled to the gate of Q1. The source of Q1 is connected to the $40V_{DC}$ supply and the drain is connected to the input of the filter F1 and the drain of Q2. The gate bias is determined by capacitor C3 and resistor R4. The gate-to-source voltage, Vgs, determines the operational point of the p-channel power MOSFET. Resistor R4 acts as a pull-up resistor for the inverter output from U3 which swings from 0 to $+12V_{DC}$. The $+12V_{DC}$ output from the inverter causes the gate to be pulled up to the $+40V_{DC}$ supply voltage and the p-channel MOSFET is off in this state with Vgs = $0V_{DC}$. The inverter then swings to $0V_{DC}$ and gate of the p-channel MOSFET is pulled down to $+28V_{DC}$ and the power FET is turned on. The gate-to-source voltage, Vgs, is $-12V_{DC}$ in this case and allows current to flow from the $+40V_{DC}$ supply at the source to the drain of the MOSFET Q1.

The MOSFETS Q1 and Q2 are never on at the same time. Q1 and Q2 are ensured to never transition at the same time by the dead-time control section of the TL598. A power supply short to ground will result if Q1 and Q2 are ever on at the same time. Likewise, Q3 and Q4 are never on at the same time. The MOSFETS Q1 and Q4 conduct simultaneously allowing the amplified signal to flow from the drain of Q1 through filter F1, the load R_L, filter F2, and through Q4 to power ground. During the other half of the square wave input audio signal, Q2 and Q3 conduct allowing the signal to flow from the drain of Q3 through

filter F2, the load R_L, filter F1, and through Q2 to power ground. Capacitors C5 and C6 are used to block any dc voltage to the load.

3. Output Filtering

Output filtering considerations are in chapter IV.

C. THE DISCRETE COMPONENT CIRCUIT

The author was unable to make the Decker circuit function properly. It is conceivable that there is an error in the circuit design or schematic. Moreover, the TL598 and the other pulse-width-modulation chips provide modulation levels of only 45% maximum. This means the power supply voltage must be double the value that would be required for a 90% pulse-width-modulation.

The following circuit is given as an alternative. It provides pulse-width-modulation up to 100%. Discrete component circuits generally use more space, but this circuit could be designed with as little as 3 chips excluding the MOSFETs and filter components.

1. Galarowicz, Hofler, and Moore Design

Discrete components consisting of a dual comparator, timer, and integrator were used to build a pulse-width-modulation section of the amplifier. The filter and MOSFET sections remained the same as the Decker circuit. The circuit design without the ouput filtering section, is shown below in Figure 2.3. The dual comparator needs to be a single supply comparator with inputs close to ground. A triangular waveform, rather than a sawtooth waveform, is used in this design for the carrier signal. The waveform is generated by an external function generator. A single audio tone is still the input modulating signal. The

triangular wave is slowed to 25kHz for this design. This waveform will be 5Vpp and have an offset of $3.5V_{DC}$. This will be the input to the non-inverting input of the U1A comparator and to the inverting input to the U1B comparator. The audio signal will be 3Vpp and have an offset of $3.5V_{DC}$. This is to ensure that there will be no over modulation and no saturation in the comparators. A modulation on the order of 66% is expected. The outputs of U1A and U1B comparators will be 180° out phase. U1A comparator will have a value close to V_{CC} when the triangular carrier wave voltage exceeds the voltage of the input sinusoid. Similarly, U1B output will have a value close to V_{CC} as the input sinusoid voltage exceeds the voltage of the triangular wave. The outputs of these two comparators will always be opposite. While the output of U1A is at V_{CC}, the output of U1B will be at ground and when the output of U1B is

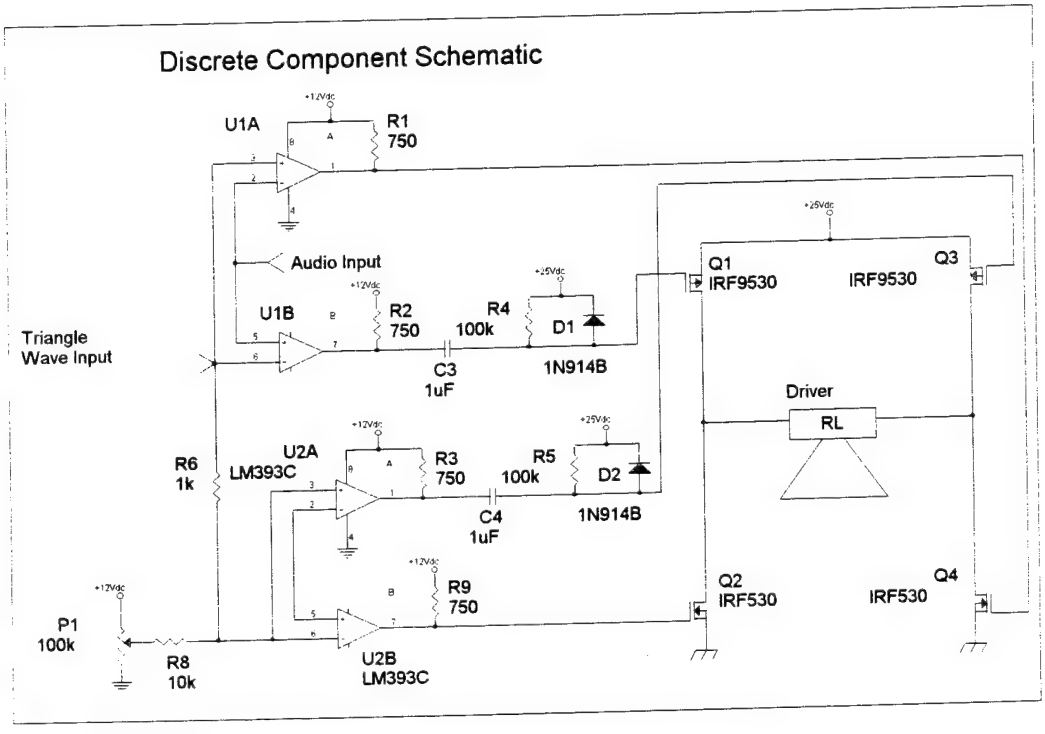

Figure 2.3 Discrete Component Schematic

at V_{CC} , the output of U1A will be at ground. The outputs of U1 are pulled high by resistors R1 and R2. The outputs of U1A and U1B are then connected to the AND gates U3A and U3D respectively. The comparators have a single power supply with pin #4 connected to ground. The small signal response time for the comparator is 1.3μseconds. The carrier frequency is reduced to minimize the effect of the response time of the comparators on the carrier waveform. The 1.3μ seconds small signal represents 3% of the triangular waveform period at 20kHz and 6.5% of the triangular waveform at 50kHz.

2. Dead-Time Generation

Dead-time is essential in this type circuit with switching power MOSFETs. A short to ground during the transition of two modulated squarewave signals is very likely with no dead-time control circuitry. A transient power supply short to ground can damage MOSFETs quickly. The following figures model dead-time generation. A Matlab program was used to model and analyze this problem. The modeling program name is PWM.M and can be found in Appendix A.

Theoretically, dead-time generation in this circuit is accomplished by boosting the DC offset of the triangular waveform by $.5V_{DC}$ at the second dual comparator chip. The triangular waveform at comparators U2A and U2B is 5Vpp and has a DC offset of 3.5V. The waveform voltage varies from $1.5V_{DC}$ to $6.5V_{DC}$, while the input sinusoid remains unchanged. Figure 2.4 shows the two comparator input signals for the U1A and the U1B chip without the extra DC offset. The figure shows the triangular carrier waveform at a frequency 20 times the input modulation signal. The triangular wave is the non-inverting input of

U1A and the inverting input of U1B. The sinusoidal signal is the non-inverting input of U1B and the inverting input to U1A. The U1A comparator output will

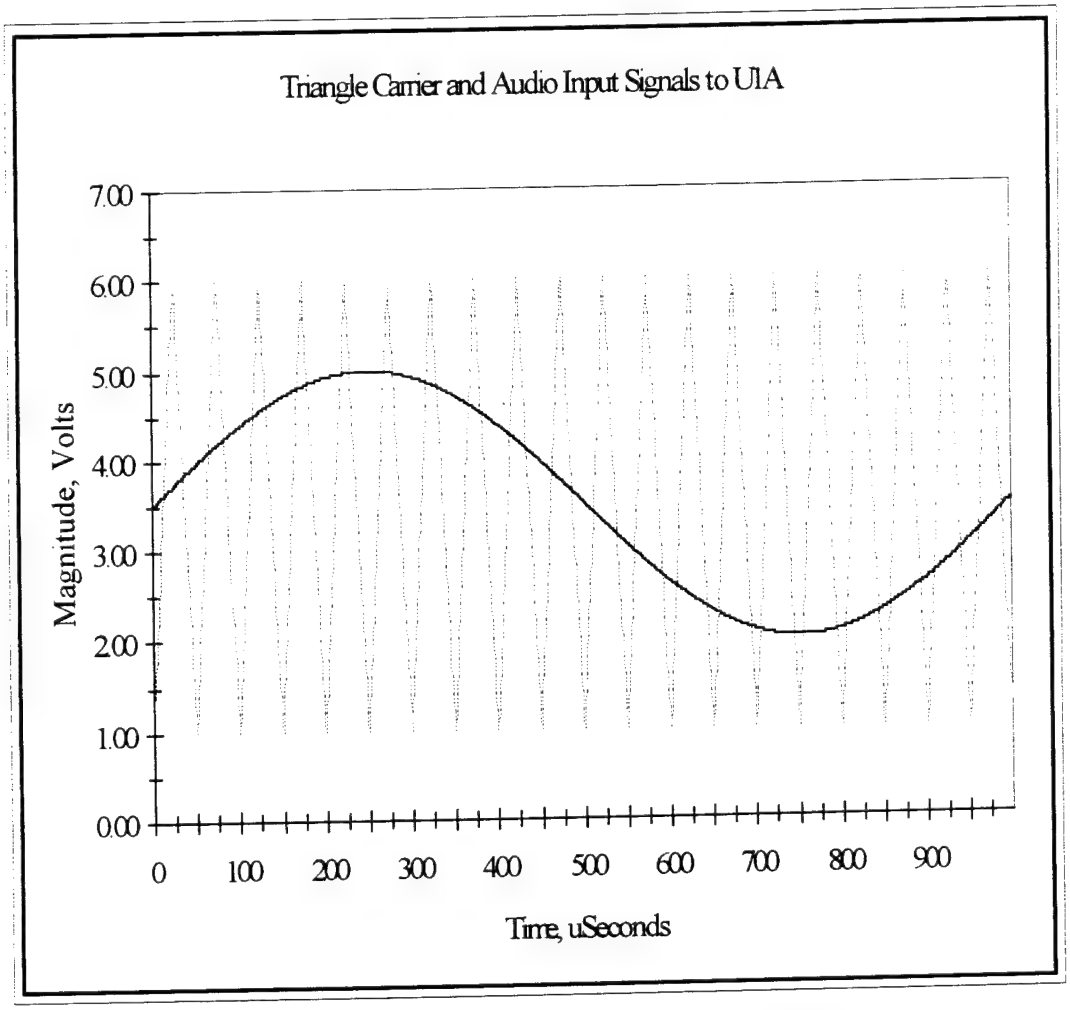

Figure 2.4 Triangle Carrier and Audio Input Signals to U1A

swing to its positive rail when the triangular wave has greater magnitude than the sinusoidal signal and swing to its negative rail when the sinusoid is greater in magnitude than the triangular wave. Figure 2.5 shows the inputs to the comparators U2A and U2B with the extra .5 V_{DC} offset. The offset is created by

an 100 kΩ potentiometer P1. The DC level shift of the carrier waveform produces a narrower positive going pulse at the output of comparator U2A. The level shift produces a wider positive going pulse at U2B.

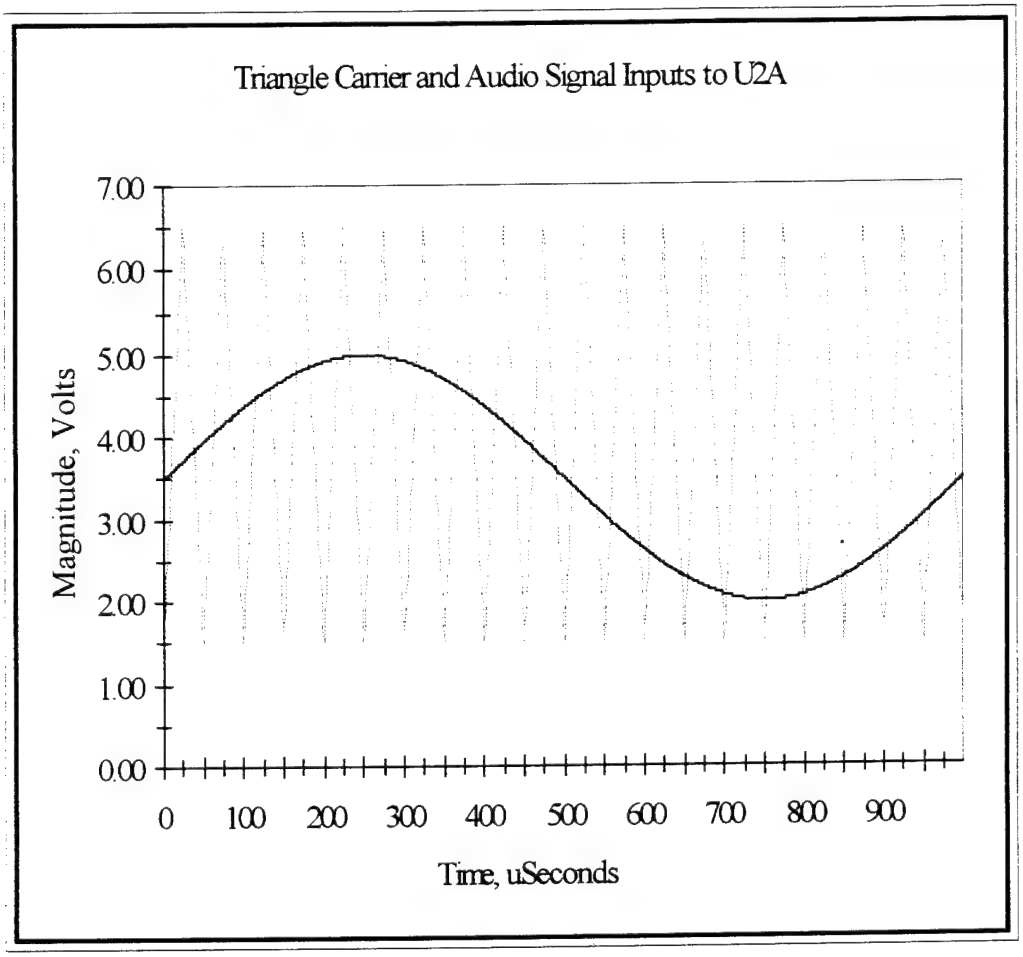

Figure 2.5 Triangle Carrier and Audio Input Signals to U2A

The dead-time generation can be seen by overlaying the pulse-width-modulation waveform outputs of comparators U1A and U2A in Figure 2.6 or by overlaying the waveform outputs of U1B and U2B in Figure 2.7. The dashed line

in Figure 2.7 is the output of comparator U2A. The dashed line can be seen to have a slightly wider positive pulse than the solid line output of U1A. The dashed line can also be seen to have a slightly narrower pulse width at $0V_{DC}$.

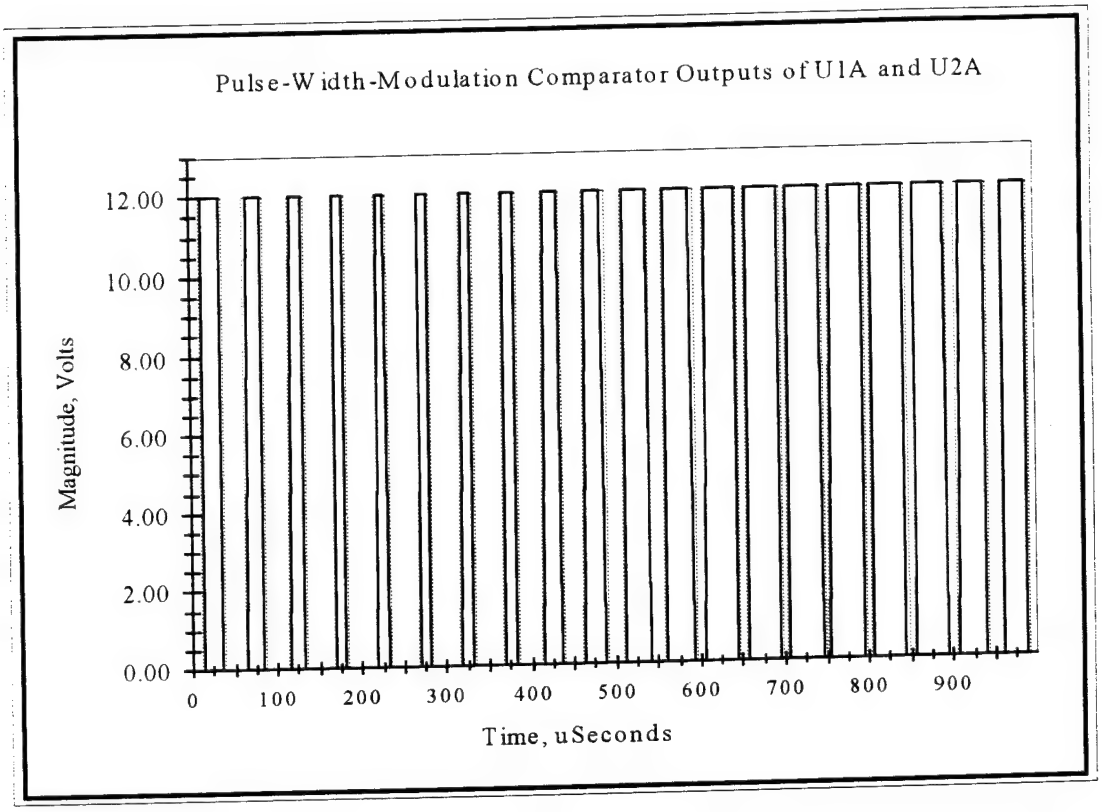

Figure 2.6 Pulse-Width-Modulated Comparator Outputs for U1A and U2A

The output of U2A is fed to the gate input of the p-channel MOSFET Q3 and the output of U1A is fed to the gate input of the n-channel MOSFET Q4. Please note Figure 2.3 for the locations of Q3 and Q4. The MOSFET Q3 conducts when the output of U2A comparator is $0V_{DC}$. The MOSFET Q4 conducts when the output of U1A comparator is $+12V_{DC}$. The small dead-time difference between the two outputs of U1A and U2A in Figure 2.6 guarantees that the two MOSFETs will never be conduct at the same time. Likewise, Figure 2.7 exhibits

the same dead-time pattern for comparator outputs from U1B and U2B. This section of the circuit operates in the same manner as the Q3 and Q4 operations described above.

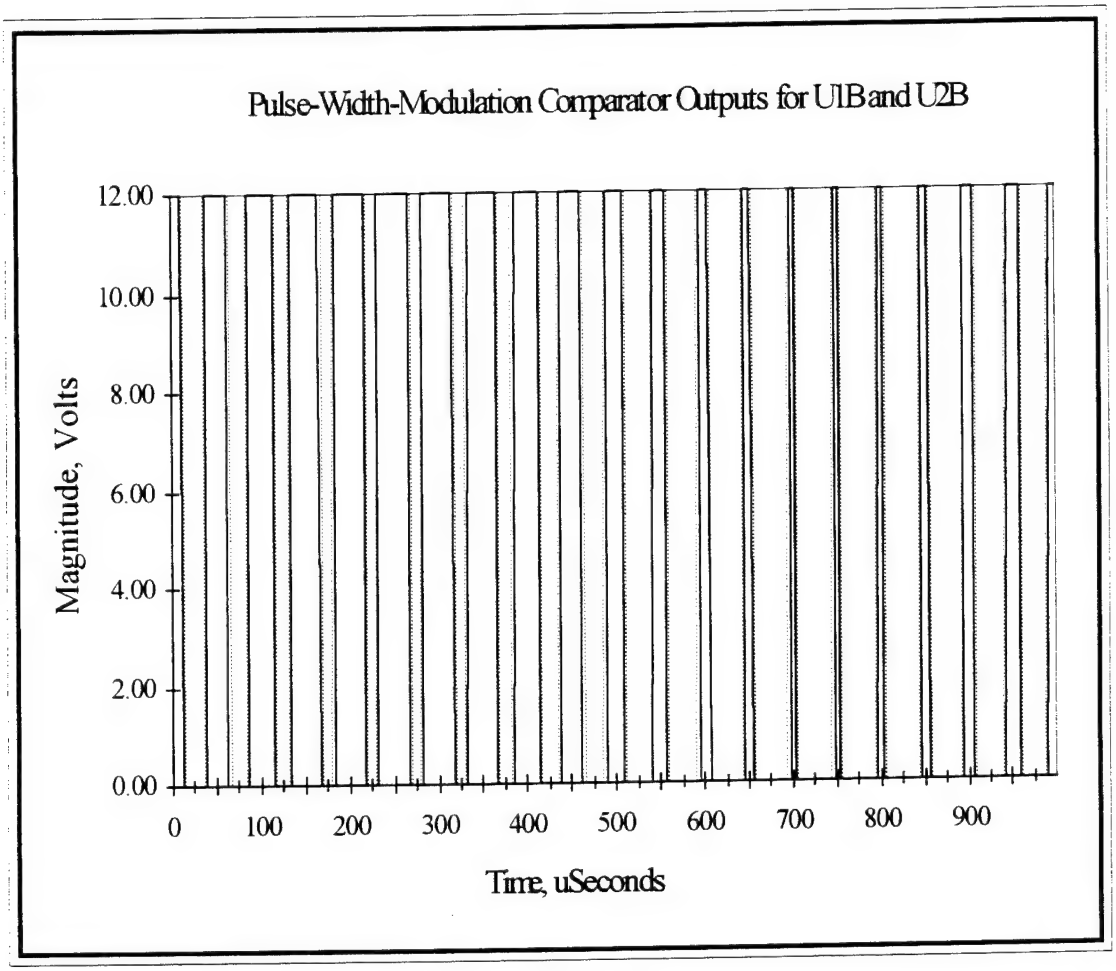

Figure 2.7 Pulse-Width-Modulated Comparator Outputs for U1B and U2B

3. Operation of the MOSFETS

The outputs of comparators U1A and U2B are directly connected to the gates of the n-channel MOSFETs Q4 and Q2 respectively. The outputs of U1A

and U2B swing from close to ground to $+12V_{DC}$. The n-channel MOSFETs are conducting during the positive pulses of U1A and U2B. The outputs of comparators U1B and U2A are capacitively coupled to the gates of the p-channel MOSFETs Q1 and Q3 respectively. Resistors R4 and R5 attempt to pull the mean gate voltage of Q1 and Q3 up to the supply voltage level. However, diodes D1 and D2 will prevent the peak gate voltage from going above the supply voltage. If the outputs of comparators U1B and U2A are high, $+12V_{DC}$, resistors R4 and R5 pull the gates of Q1 and Q3 to $+25V_{DC}$. In this state, the p-channel MOSFETs are shut off. If the outputs of comparators U1B and U2A are low, $0V_{DC}$, the gates of Q1 and Q3 voltage level drop to $+13V_{DC}$. In this state, the p-channel MOSFETS are conducting. The two p-channel MOSFETs are never on or off simultaneously. MOSFETs p-channel Q1 and n-channel Q4 conduct and turn off at exactly the same time. When conduction occurs in Q1 and Q4 a path is generated from the $+25V_{DC}$ power supply through filter F1, load R_L, filter F2, and to power supply ground. Likewise, MOSFETs Q3 and Q2 conduct and turn off at the same time generating a path from the power supply, through filter F2, load R_L, filter F1, and to power supply ground.

III. POWER CALCULATIONS

A. INTRODUCTION

The following power calculations represent the theoretical power to be supplied by the switching power amplifier design. A rough calculation will be conducted based on the ideal values of the resistance for the power MOSFETs, inductors, and discrete components. Another calculation will be made using the resistance values from the data sheets for the power MOSFETs, the measured resistance in the inductors at discrete frequencies, and the power consumption specified in the data sheet for the discrete integrated circuits.

B. THE PERFECT WORLD

For this case, the calculation of power for the switching power amplifier is simple and straightforward. The assumptions made are:

MOSFETs dissipate no power;

Inductors have no resistance;

Integrated circuit consume no power.

These assumptions allow a standard, quick calculation for a 100% efficient power amplifier to be made. Power can be calculated using the above assumptions and the following equation

$$P = I_L^2 R_L = 2^2 \times 8 = 32 \text{ Watts} \qquad (3.1)$$

where I_L = 2 Amperes RMS. This is a reasonable result. The author will compare this theoretical calculation with the actual circuit's power consumption.

C. POWER CALCULATIONS WITH THEORETICAL LOSSES

The data sheets of the power MOSFETs, comparator chips, and measurements of the inductor resistance, provide calculations for the power losses within these devices. These results are totaled and added to the ideal theoretical power given in equation 3.1. The actual power measurements in Chapter V will be the final measurement of how the theoretical calculations approximate the actual switching power amplifier system.

1. Power Losses in the MOSFETs

The power MOSFETs have inherent resistances when conducting. These resistances vary depending on the MOSFET chosen. The p-channel 9530 device and the n-channel 530 device are the power MOSFETs chosen for this amplifier. The p-channel 9530 transistor has a maximum on-resistance, R_D, given in the data sheet as 0.3 Ohms. The n-channel 530 device has a maximum on-resistance, R_D, of 0.16 Ohms. These are the worst case maximum values. It is possible that the resistances may be lower. The inductors at this point are assumed to have no resistance. For a fixed output power, the total power consumption of the system has been increased because of the insertion of 2 resistors in the line to the load. Only one channel of the amplifier is conducting at a single instance, thus the power losses calculations is needed for only one channel at time. One p-channel MOSFET and one n-channel MOSFET exist in each channel. The power losses for the system due to the MOSFETs resistances can be found from

$$P = I_L^2 (R_{N2} + R_{P1}) = 1.8 \text{ Watts} \qquad (3.2)$$

where R_{P1} is the on-resistance of the first p-channel MOSFET and R_{N2} is the on-resistance of the second n-channel MOSFET. The resistance values are worst case values; however, there are large transient currents in the MOSFETs at the switching frequency and higher frequencies will increase the actual power losses. The amplifier performance could be enhanced by using MOSFETs with lower resistance values.

2. Power Losses in the Inductors

The inductors were hand-wound so no data sheets were available. The inductors resistances were measured using an impedance analyzer. The real portion of the impedance was recorded for several discrete frequencies. The measurements are in the range of 50Hz to 100kHz. The oscillator output level was set to 1 Volt. The results of these measurements are listed in Table 3.1.

freq (Hz)	L_1-1 (Ohms)	L_1-2 (Ohms)	L_2-1 (Ohms)	L_2-2 (Ohms)
50	.017	.016	.009	.007
100	.021	.020	.010	.008
500	.049	.051	.015	.014
1000	.085	.090	.023	.022
5000	.394	.421	.088	.088
10000	.800	.860	.177	.182
50000	4.43	4.51	1.16	1.26
100000	9.0	8.9	2.91	3.23

Table 3.1 Inductor Resistance vs Frequency

The inductors become very resistive at the higher frequencies. The resistance values corresponding to 500Hz, the audio input frequency, will be used to calculate the power losses in the inductors. The MOSFET resistance values will be included to give a rough estimate of the total power losses of the system. All four of the inductors will conduct during the operation of the amplifier. This would add four resistance values to the power calculation. An equivalent circuit is shown in Figure 3.1.

Seven resistive values are in the equivalent circuit. The load R_L is the dominant value, but the inductor resistances and MOSFET resistances make a contribution. The estimated total theoretical power loss of the switching power

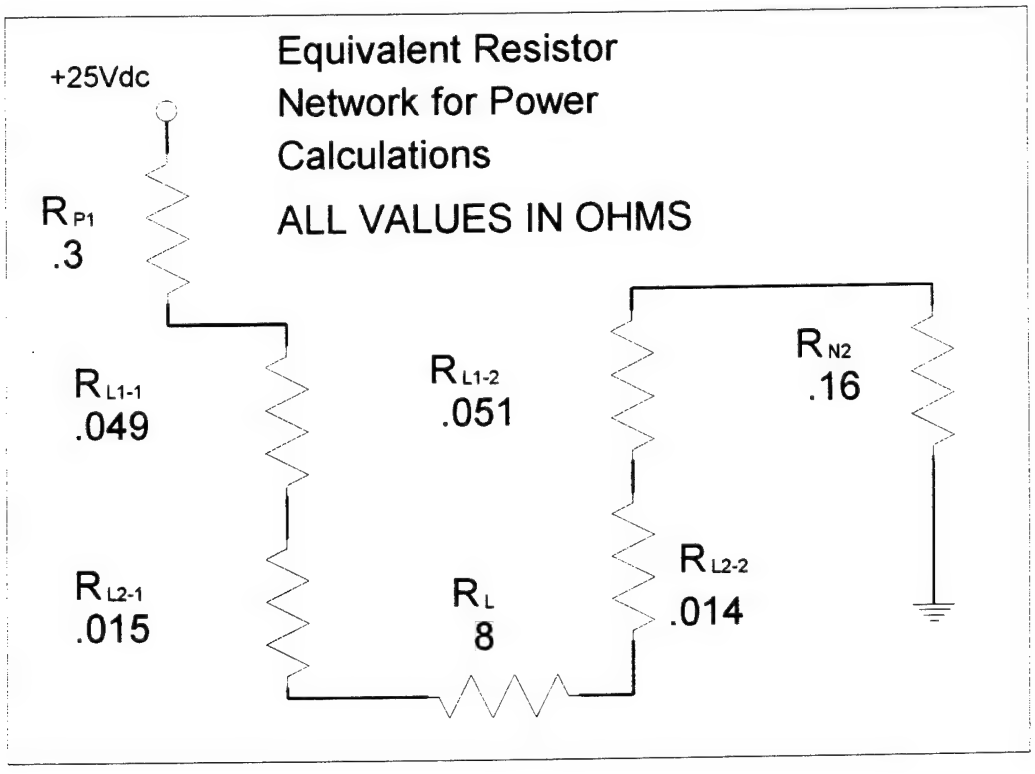

Figure 3.1 Equivalent Resistor Network for Power Calculations

amplifier system can be found using the equation

$$P = I^2_L (R_{P1} + R_{L1-1} + R_{L2-1} + R_{L2-2} + R_{L1-2} + R_L + R_{N2}) = 2.3 \text{ Watts} \qquad (3.3)$$

where $R_L = 8\Omega$, $R_{L1-1} = .049\Omega$, $R_{L2-1} = .015\Omega$, $R_{L1-2} = .051\Omega$, $R_{L2-2} = .014\Omega$, $R_{P1} = .3\ \Omega$, and $R_{N2} = .16\Omega$. This gives a rough estimate of the power loss due to inductor and MOSFET resistances. The loss due to the inductors is approximately .5 Watt. Again, there will be large components of the current in the L_1 inductors at the switching frequency that are ignored here, so the actual losses will be higher. The calculated losses for the L_2 inductors should be accurate since most of the switching components would have been removed.

3. Power Losses in the Comparator Chips

The pulse-width-modulation circuit running the MOSFET and the filter section cannot be neglected in this calculation. The comparator chips used in the circuit have power dissipation specifications of 192mW for the 8 pin molded dip package. This is the worst case. The circuit utilizes two of these chips so it will be assumed that 400 mW of power will be dissipated in the comparators. The final estimate for theoretical power loss will be 2.7 Watts. This power is within design specifications given to the author at the start of this research. The theoretical value for the power losses will be compared to the actual measured value for power losses in the results section of this thesis. No power calculations were carried out with respect to the temperature variation.

D. CALCULATED EFFICIENCY

An estimate of the efficiency of the system can be modeled by the following equation:

$$E = \frac{P_{OUTPUT}}{P_{INPUT}} \times 100 = \frac{32.0}{34.7} \times 100 = 92.2\% \qquad (3.4)$$

The calculated theoretical efficiency E is well within the parameters of this thesis. However, Equation 3.4 represents only a rough estimate. This value will be compared to the measured efficiency of the circuit in Chapter V.

IV. THE BUTTERWORTH FILTER

A. INTRODUCTION

The Thermoacoustic Refrigerator is run at a single frequency in the range of 300Hz to 700Hz. Therefore, a filter with low-pass characteristics is used to filter out the modulation frequency of 50kHz. The load impedance R_L is presently not known. The value is estimated to be in the range of 4-8 ohms. The filter chosen must be easily adapted to match the exact impedance of the driver for maximum efficiency. A filter with a cutoff frequency of 1kHz and a rolloff of 18dB per octave is the ideal theoretical starting point for the design of this filter, but cost, size, and number of components needs to be limited. A low-pass passive Butterworth LC filter network of order N=3 was selected for its maximally flat property in the passband region and its steep roll-off in the stopband. A Matlab Program B3PFILPG.M was written to allow the user to specify the load resistance and other variables for calculating the components of a third order Butterworth filter. This allows for quick and easy modifications for different load characteristics.

B. THE TRANSFER FUNCTION

The roots to solve the transfer function for a Butterworth filter reside only in the denominator. These roots, called poles, are signified by the symbol 'X' in the s-plane. Figure 4.1 shows the pole locations for a low-pass Butterworth filter of order N=3. Note that there are 6 poles in the figure. The poles occur as complex conjugate pairs. The cutoff frequency ω_c is normalized to 1 in this s-

plane plot. The numerator solutions, if there were any, would be called zeros and be signified by the symbol '0' in the s-plane.

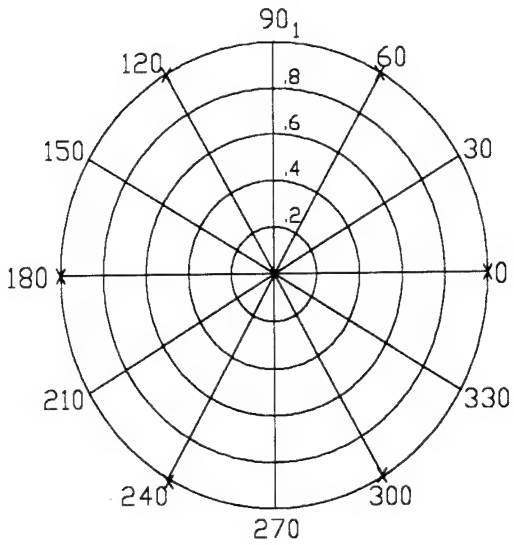

Figure 4.1
Pole Locations S-Plane

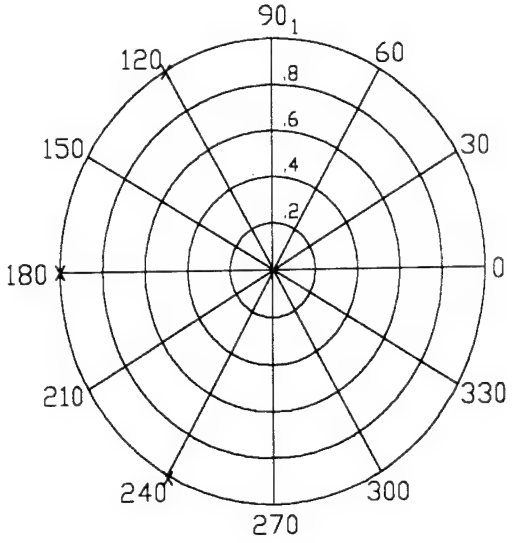

Figure 4.2
Stable Pole Locations

To construct a stable and causal transfer function for the Butterworth filter, only one pole from each complex conjugate pair is selected. See Figure 4.2. The pole of a complex conjugate pair is selected if it lies in the left-half of the s-plane. Oppenheim, Willsky, and Young [Ref. 4] give four generalities in placement of the poles in the s-plane for a low-pass Butterworth filter:

1. There are 2N equally spaced poles by angle on a circle of radius ω_c.
2. No pole ever lies on the $j\omega$-axis. A pole can lie on the σ-axis when the order of the filter is odd, but not when the order of the filter is even.
3. The angular spacing between poles is π/N radians, where N = order of the filter.

4. The poles occur as complex conjugate pairs.

The transfer function for the third order Butterworth filter section of the switching power amplifier is of the form

$$T(s) = \frac{N(s)}{D(s)} = \frac{D}{As^3 + Bs^2 + Cs + D} . \tag{4.1}$$

where $s = j\omega$.

For a third order Butterworth, the coefficients are equated to:

$$T(s) = \frac{N(s)}{D(s)} = \frac{\omega_c^3}{s^3 + 2\omega_c s^2 + 2\omega_c^2 s + \omega_c^3}. \tag{4.2}$$

Setting the denominator D(s) = 0 and solving for the roots of the equation yields the pole locations needed for a third order Butterworth filter. The solutions for the poles in the above equation lie on a circle of radius ω_c at angles of $2\pi/3$, π, and $4\pi/3$. The poles in the left-half plane are used to furnish a stable, causal system. The theoretical roll-off for the third order Butterworth filter is 18dB per octave in the stopband. The order of the transfer function is N=3. Note that the poles are spaced by π/N radians. The poles for a Butterworth filter with N=3 are situated on the pole-zero plot shown in Figure 4.1.

The pole locations can be found using the following equations:

$$|s_p| = \omega_c \tag{4.3}$$

$$\text{ang } s_p = \frac{\pi(2k+1)}{2N} + \frac{\pi}{2}, \quad k \text{ an int eger} \tag{4.4}$$

The pole locations for a third order Butterworth filter are located at $2\pi/3$, π, and $4\pi/3$ for k = 0, 1, and 2 respectively. The poles are equally spaced by radian angle.

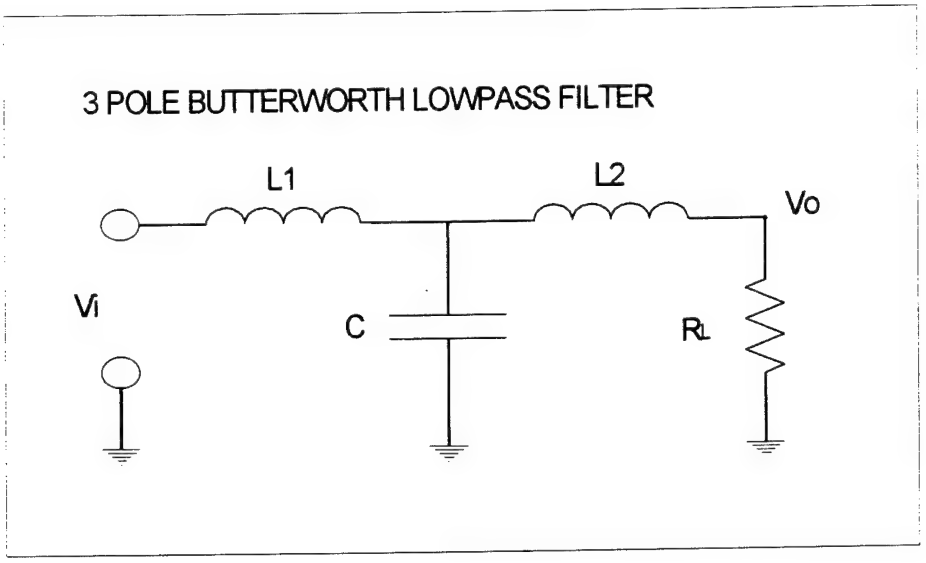

Figure 4.3 Three Pole Lowpass Butterworth Filter

Solving the nodal equations for the circuit schematic shown in the Figure 4.3 produces the following reduced gain equation:

$$\frac{V_o}{V_i} = \frac{R_L}{L_1L_2CS^3 + L_1CR_LS^2 + (L_1 + L_2)S + R_L} \tag{4.5}$$

Dividing by the factor L_1L_2C, results an equation of the same form as equation 4.2.

$$\frac{V_o}{V_i} = \frac{\dfrac{R_L}{L_1L_2C}}{S^3 + \dfrac{R_L}{L_2}S^2 + \dfrac{(L_1 + L_2)}{L_1L_2C}S + \dfrac{R_L}{L_1L_2C}} \tag{4.6}$$

Equating the coefficients of equations (2) and (6) results in the following

$$2\omega_c = \frac{R_L}{L_2} \tag{4.7}$$

$$2\omega_c^2 = \frac{L_1 + L_2}{L_1 L_2 C} \tag{4.8}$$

$$\omega_c^3 = \frac{R_L}{L_1 L_2 C} \tag{4.9}$$

where the variables are as follows:

R_L = Load resistance of a driver in Ohms.

ω_c = Cutoff frequency in radians per second.

L_1 = Inductance of first inductor in Henries.

L_2 = Inductance of second inductor in Henries.

C = Capacitance of shunt capacitor in Farads.

Given three equations with five unknowns, the filter can be designed if two of the unknowns are specified. The Matlab program B3PFILPG.M was written to help design a three pole low-pass Butterworth filter. The frequency response can then be calculated to insure a flat response at the input audio frequency of 300Hz to 700Hz with a very large dropoff to eliminate the switching modulation frequency of ≈ 50kHz.

C. B3PFILPG.M

The acronym B3PFILPG.M stands for Butterworth 3 Pole FILter ProGram. The program uses five variables: rl = R_L, fc = $\omega_c/2\pi$, l1 = L_1, l2 = L_2, and c = C. The user must specify two of the five unknown variables to input.

The program calls one of four other programs depending on the user's selection in the main menu. These programs can be found in Appendix A. The program filenames that B3PFILPG.M calls are as follows:

FILTPROA.M Called if user wishes to input the load resistance R_L and the cutoff frequency fc.

FILTPROB.M Called if user wishes to input the load resistance R_L and the shunt capacitance C.

FILTPROC.M Called if user wishes to input the load resistance R_L and the second inductance L_2.

FILTPROD.M Called if user wishes to input the load resistance R_L and the first inductance L_1.

The author decided that since the impedance of the driver can be measured, the load resistance is not calculated by the program. The impedance of the driver is one of the two parameters that must be specified by the user. B3PFILPG.M calculates the remaining three variables and plots the frequency response of the filter with its new values. The plots are then stored in a meta graphics file for later printing on a high resolution laser printer. The program returns to the main menu after dumping the plots to a single graphics file specified by the user. After exiting the program the user can print the plot by

typing **grafl filename** at the DOS prompt. No extension is necessary since Matlab assumes it ends with .met. Each program was tested with the load resistance = 8Ω. The first program allows the user to input any cutoff frequency. The chosen cutoff frequency was 10kHz. The program then returned the following calculated values for L_1, L_2, and C:

$$L_1 = 191\ \mu H$$

$$L_2 = 63.6\ \mu H$$

$$C = 2.65\ \mu F$$

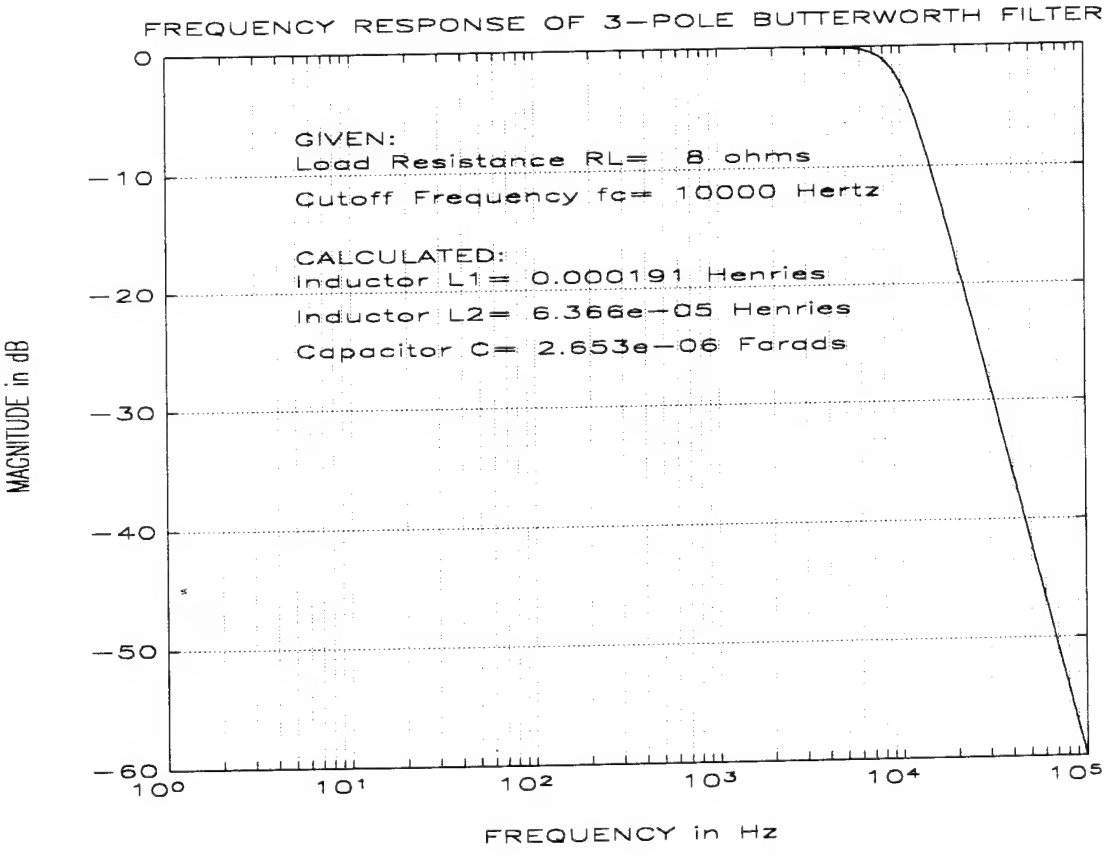

Figure 4.4 Calculated Frequency Response of Third Order Lowpass Butterworth Filter Given the Load Resistance and the Cutoff Frequency

A plot was generated and stored in the filename specified by the author as run1. Grafl then plotted the results to a laser printer. The results are shown in Figure 4.4. The program then returned the user to the main menu. Figure 4.4 shows good agreement with the characteristics of the theoretical low-pass Butterworth filter.

The second selection was then chosen from the main menu. The program prompts the user to input the load resistance R_L, the shunt capacitance C, and a new filename for the graphics file. Again, 8Ω was entered for R_L and 2.65 μF was entered in lieu of the cutoff frequency. Note that this capacitance is a result from the first run of the program, and will verify whether the cutoff frequency and inductance values remain consistant to the third significant digit. The following values were generated by the second run of the program:

$$L_1 = 191\ \mu H$$

$$L_2 = 63.6\ \mu H$$

$$fc = 10.01\ kHz$$

These agree with the first run of the program within 3 significant figures. The results of the plot are shown in Figure 4.5. The program was run two more times. Runs 3 and 4 followed with each of the respective inductor values being entered as the second variable. The load resistance was kept as the lone constant. The values of the inductors were taken from the first run of the program. The capacitance and cutoff frequencies were then calculated by the program. The results again agree with the two previous runs of the program. The resulting calculations agree with the other runs of the programs within 3 significant figures. The plots and results of the program runs can be found in the Appendix.

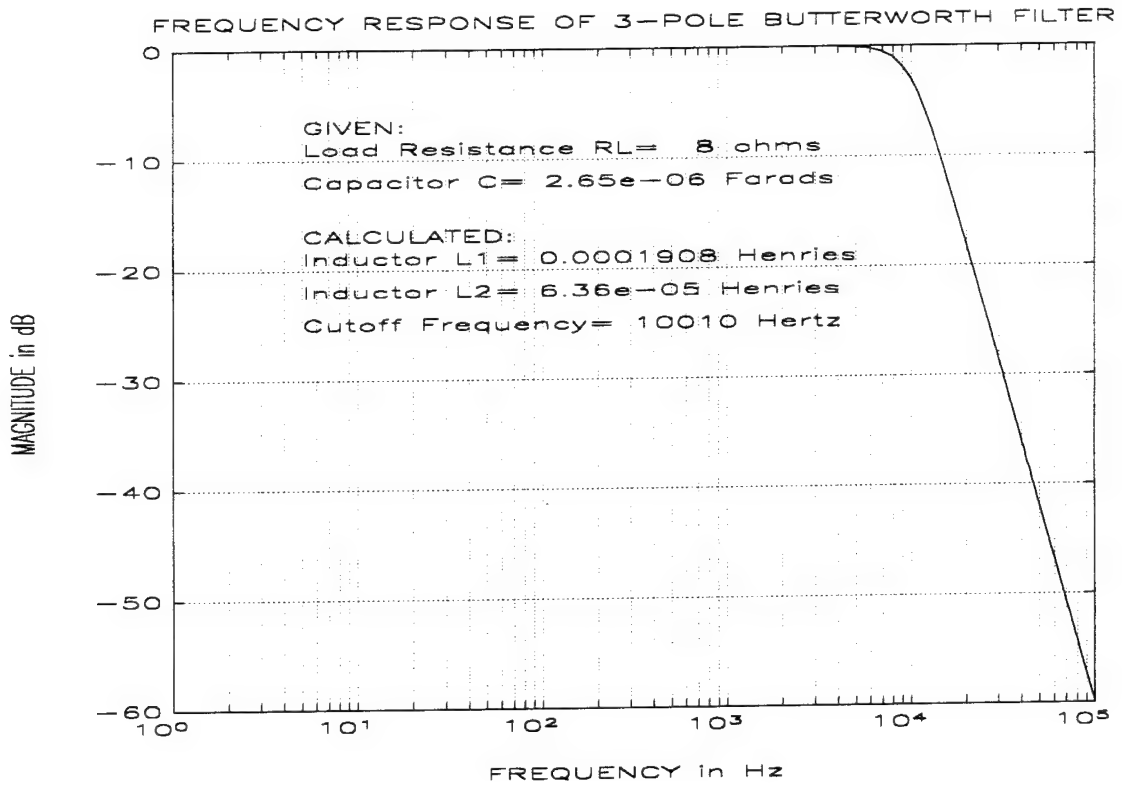

Figure 4.5 Calculated Frequency Response of Third Order Lowpass Butterworth Filter Given the Load Resistance and the Capacitance

D. BUILDING THE FILTER

The program B3PFILPG.M was used to calculate the inductance values and the cutoff frequency for the 3-pole low-pass Butterworth filter to be used in the output section of the power amplifier. The inductors L_1 and L_2 were hand wound to the values specified by the program given a load resistance $R_L = 8\Omega$ and a shunt capacitance of 3.3 μF. The capacitor was chosen as the second program parameter since it is easier to build inductors of a specified value than a

capacitor of a certain capacitance. The capacitor chosen was 3.3 μF with a working voltage of 100VDC. This is a readily available item. The program calculated the following values for the inductors and cutoff frequency:

$$L_1 = 237.6\ \mu H$$

$$L_2 = 79.2\ \mu H$$

$$f_c = 8.038\ kHz$$

The cutoff frequency is not critical other than it should be low enough for the filter to reject the 50kHz switching frequency in the stopband. The frequency

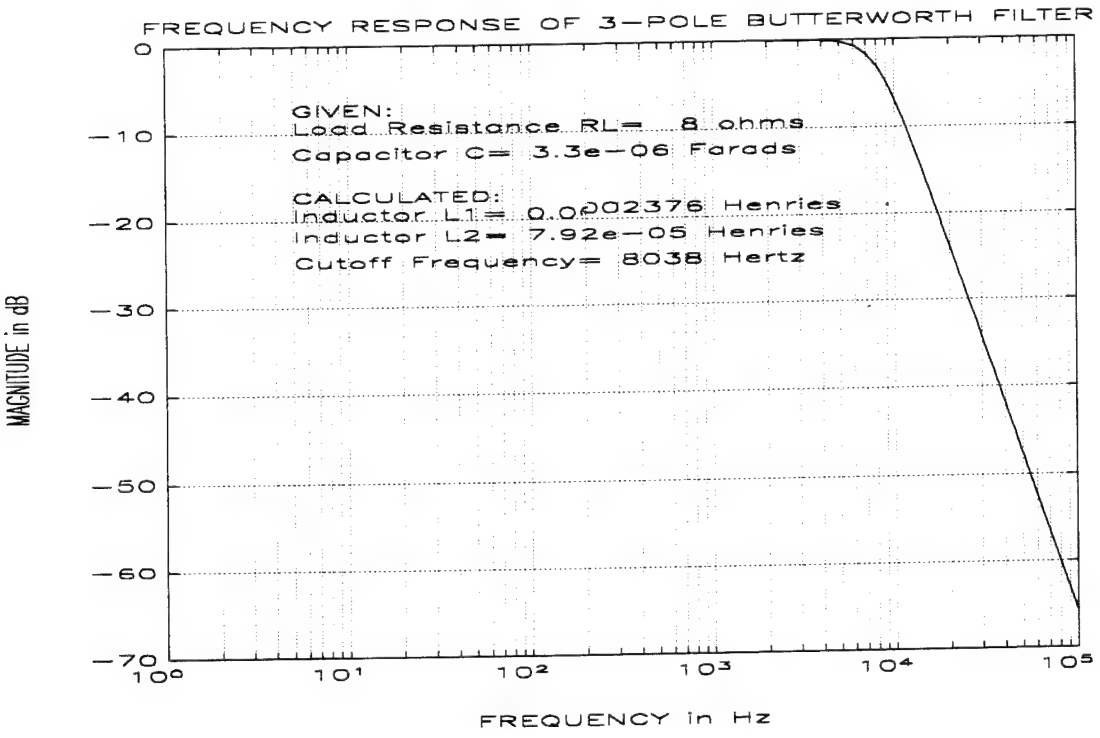

Figure 4.6 Calculated Frequency Response of Third Order Lowpass Butterworth Filter Given the Load Resistance and the Capacitance

response for a filter with these parameters is shown in Figure 4.6. The frequency response in Figure 4.6 shows the -3dB corner frequency to be approximately

8kHz. The stopband shows a -47dB drop in magnitude at the 50kHz carrier frequency. Close inspection of the frequency response in the stopband shows an 18dB drop from approximately 15kHz to 30kHz. This agrees theoretically with the 18dB rolloff in the stopband for a 3-pole Butterworth low-pass filter.

The inductors were wound using a ferrite torroidal core. The number of turns needed for the above calculated values can be found using

$$\#\ of\ turns = 1000\sqrt{\frac{desired\ L\ (mH)}{A_L\ (mH/1000)}}. \tag{4.10}$$

The A_L value for this material is given as 73.3(mH/1000). This formula produced 13 turns for L_1 and 7 turns for L_2 for the calculated values above. The inductors were then wound and their inductances measured using an

freq (Hz)	L_1-1 (mH)	L_1-2 (mH)	L_2-1 (mH)	L_2-2 (mH)	C1 (μF)	C2 (μF)
5	.3	.3	.2	.2	3	3
50	.25	.25	.08	.09	3.3	3.3
500	.239	.249	.078	.091	3.32	3.28
5000	.238	.248	.077	.091	3.310	3.261
50000	.233	.243	.077	.089	3.319	3.272
100000	.221	.231	.074	.085	3.457	3.403
200000	.219	.230	.074	.084	4.302	4.219

Table 4.1 Inductance vs Frequency

impedance analyzer over a range of frequencies. The inductors were labeled L_1-1, L_1-2, L_2-1, and L_2-2 for matching purposes. The capacitors were also measured using the impedance analyzer and labeled C1 and C2. The results of these measurements are in the Table 4.1. The measured values from the 500Hz row of Table 4.1 were inserted into the author's Matlab™ Program PABOD.M to plot the frequency response of the filter using the measured values. Capacitor C1 is used with inductors L_2-1 and L_2-2 to form the filter F1, shown in the schematic of Figure 4.3. Capacitor C2 is combined with inductors L_1-1 and L_1-2 to form the filter F1.

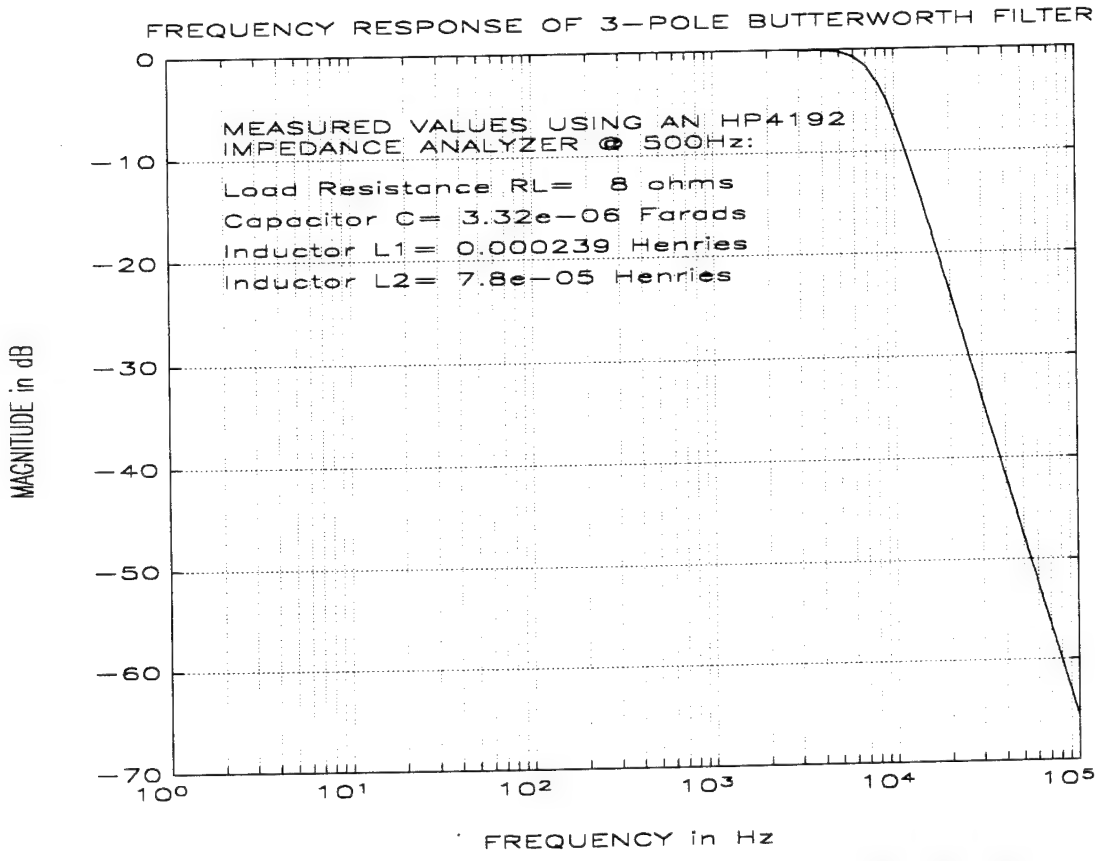

Figure 4.7 Measured Frequency Response of Butterworth Filter F1

The frequency response plots for filters F1 and F2 are shown in Figures 4.7 and 4.8 respectively. The cutoff frequencies of each plot are observed to be approximately equal to 7.5kHz. The plots still show a maximally flat response in the passband and a sharp rolloff in the stopband. The magnitude at the 50kHz carrier signal frequency shows an attenuation of -47dB and -44dB respectively. These magnitude values will ensure the carrier frequency is suppressed at the load. These filter frequency responses are within the specifications set for the output section of the power amplifier. The roll-off is approximately 18dB per octave. This agrees theoretically with the rolloff for a typical 3 pole filter.

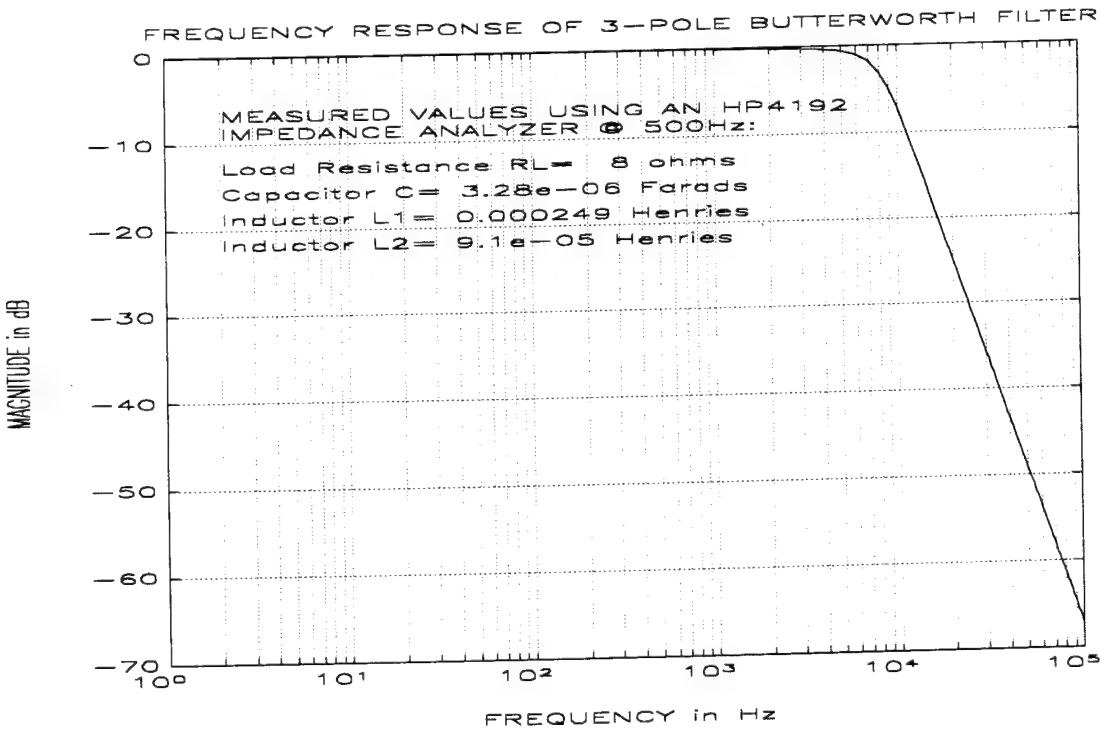

Figure 4.8 Measured Frequency Response of Butterworth Filter F2

The impedance analyzer was then used in the gain-phase mode of operation to physically measure the frequency response of the filters F1 and F2 after assembly. The filters were driven by a 1 volt RMS sine wave from 10Hz to 100kHz. The settings for the impedance analyzer were as follows:

OSC LEVEL:	.5Volts
LOG SWEEP:	ON
AVERAGE:	ON
START FREQ:	10Hz
STOP FREQ:	100kHz
STEP FREQ:	100Hz
dBV Mode:	ON.

Dr. Hofler's data acquistion program for the impedance analyzer was used to create the data file containing the results of this measurement. The ASCII file provided by the program was then downloaded into the graphing program to plot the data. The first plot is the frequency response of the Butterworth filter F1 and the second plot is the frequency response of the Butterworth filter F2, Figures 4.9 and 4.10, respectively. Comparing the first plot with that of the calculated and the measured plot in Figure 4.7, the theory and experimentally measured plots agree very closely. The plots are maximally flat in the passband and have steep roll-off in the stopband. The cutoff frequency, as measured from the plot below, can be seen to be $\approx$ 7.5kHz. The filter works as theory predicts and concurs with the experimentally measured values of the discrete components used in the design of this filter. The second plot below also shows

good agreement with that of the theoretical and measured plots of Figures 4.6 and 4.7. The cutoff frequency as seen from the plot is ≈ 7kHz. The filter section is now built and can be incorporated into the power amplifer output section.

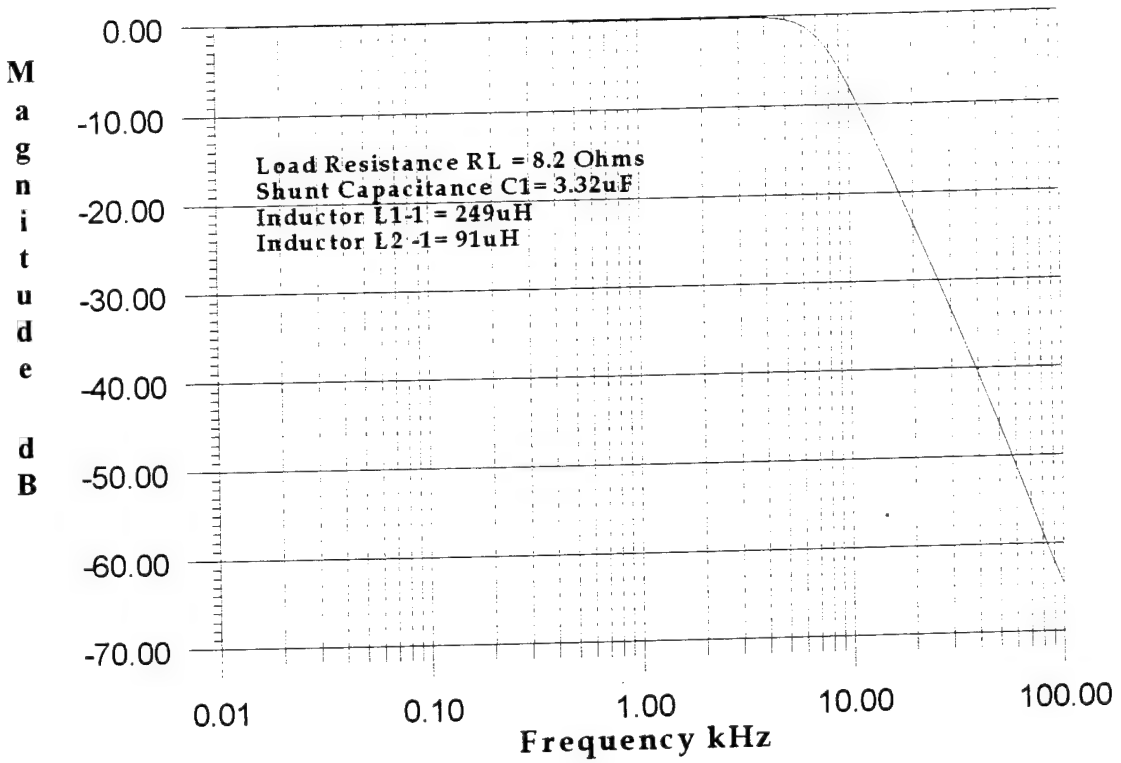

Figure 4.9 Measured Frequency Response of Butterworth Filter F1

E. EFFICIENCY OF THE FILTER

The efficiency of the filter needed to be measured for calculation of losses within the power amplifier system. The real portion of its impedance can be measured using an impedance analyzer. The load resistance R_L can then be subtracted to give a reasonable estimate of the losses occurring within the filter. Low level current measurements were taken through the filter with R_L attached. The real part of the impedance was found to vary from 8.28Ω at 300Hz to 10.16Ω

at 10kHz. The load resistor was also measured over this range and was found to have a constant value of 8.03 Ω. The efficiency of the filter at the input audio signal of 500Hz is calculated to be 96%. The filter becomes highly resistive in the kHz range. These measurements were taken from 300Hz to 10kHz.

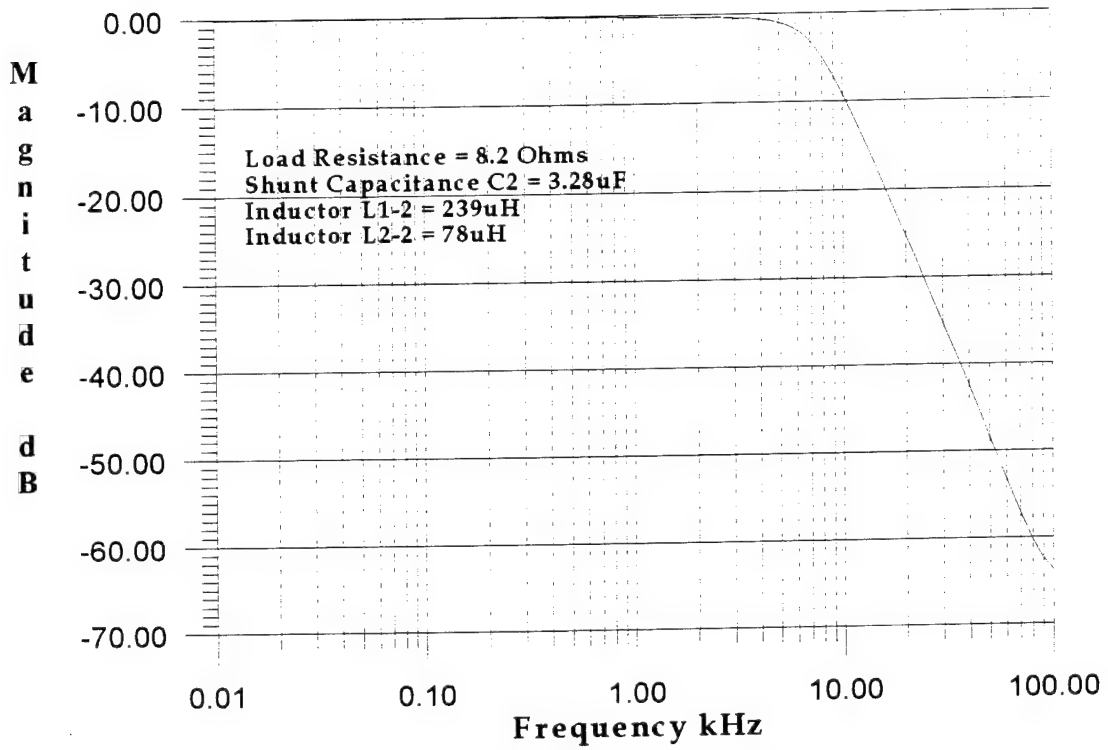

Figure 4.10 Measured Frequency Response of Butterworth Filter F2

V. MEASUREMENT RESULTS

A. PULSE-WIDTH-MODULATION MEASUREMENTS

Pulse-width-modulation was the most successful section of this research. The outputs from the comparators provided a modulation of 0 to 100% depending on input amplitude. Figure 5.1 shows the outputs of the comparators with dead-time and a triangular wave frequency of 20kHz and an input

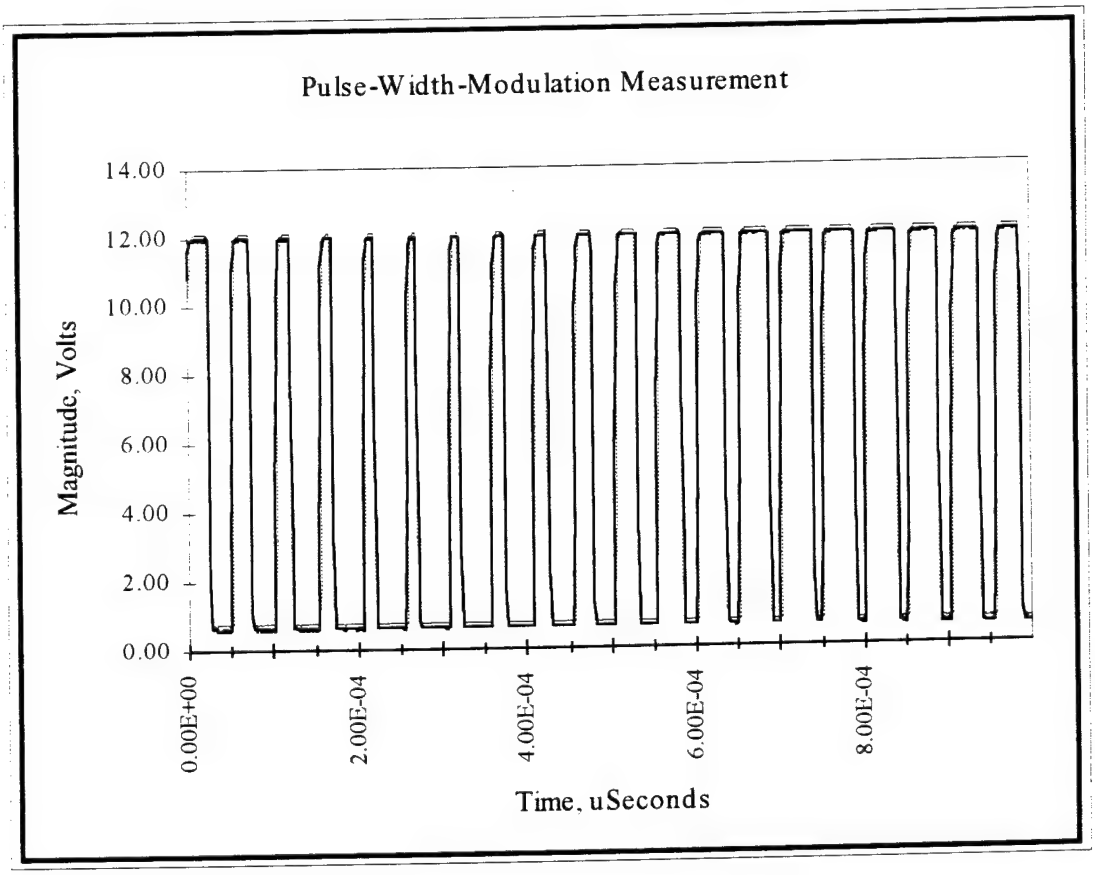

Figure 5.1 Pulse-Width-Modulation Measurement

sinusoidal signal of 1kHz at approximately 66% modulation. Figure 5.1 can be compared to the theoretical result in Figure 2.7. The actual output agrees quite well with theory with the exception that the squarewaves tend to have some overshoot and rounding of the comparator outputs. If the input audio signal amplitude and its offset were the same as the triangular wave, we would have 100% modulation. This could cause some clipping and overlap problems. In this experiment the triangular wave input was 6Vpp with $3.5V_{DC}$ offset. The input audio signal was set at 4Vpp with $3.5V_{DC}$ offset. If these were the only inputs necessary for the circuit we would have 66% modulation. The dead-time control circuit, however, shifts the triangular wave up by $.5V_{DC}$ on the second set of comparators and it was necessary to reduce the amplitude of the input audio signal by .5Vpp. The offset remained unchanged. The percentage of modulation was measured for varying input sinusoid amplitudes. The function generator used was limited to 10Vpp. The offset had to be adjusted down so that a higher percentage of modulation could be measured. The percentage of modulation was measured using an oscilloscope. The maximum variance of the pulse width was divided by the maximum pulse width to get a percentage of modulation. The accuracy of these measurements is only 5% since the measurements are done visually. The experimental maximum for modulation was 88%. The triangular wave was set for 35kHz and the input sinusoidal signal was set at 1kHz for the measurements. The comparator chip circuit gave a percentage of modulation from 0 to approximately 100%. The dedicated pulse-width-modulation chips would only modulate to a measured 45%. The measurements taken from the comparators proved that the comparator chip circuit is superior in this respect. Table 5.1 shows the results of these measurements.

Input Amp RMS Volts	Triangle Amp RMS Volts	Input Offset VDC	Triangle Offset VDC	Percent of Modulation (%)
.207	3.33	3.5	3.5	11
.810	3.33	3.5	3.5	34
1.22	3.33	3.5	3.5	47
1.82	3.33	3.5	3.5	63
2.42	3.33	3.0	3.0	73
2.62	3.33	3.0	3.0	78
2.82	3.33	3.0	3.0	80
3.01	3.33	2.5	2.5	85
3.08	3.33	2.5	2.5	88

Table 5.1 Measurements of Comparators

The modulated waveform overlaps and distorts at anything above 88% modulation.

The dead-time control section operated effectively. The DC offset voltage sufficiently offset the input triangular waveform by .5VDC on the second set of comparators. The dead-time was measured using a digital oscilloscope. The maximum dead-time measured was 1μSec on either side of the pulse. Figure 5.2 was magnified to measure the dead-time of a single pulse. Figure 5.2 shows the maximum dead-time achievable by this system. The minimum dead-time available is zero. The pulses transition at exactly the same time when the dead-

time is zero. A time measurement can be taken from the figure. Each minor division on the x-axis represents 2μSec of time. At the rising edge the dead-time

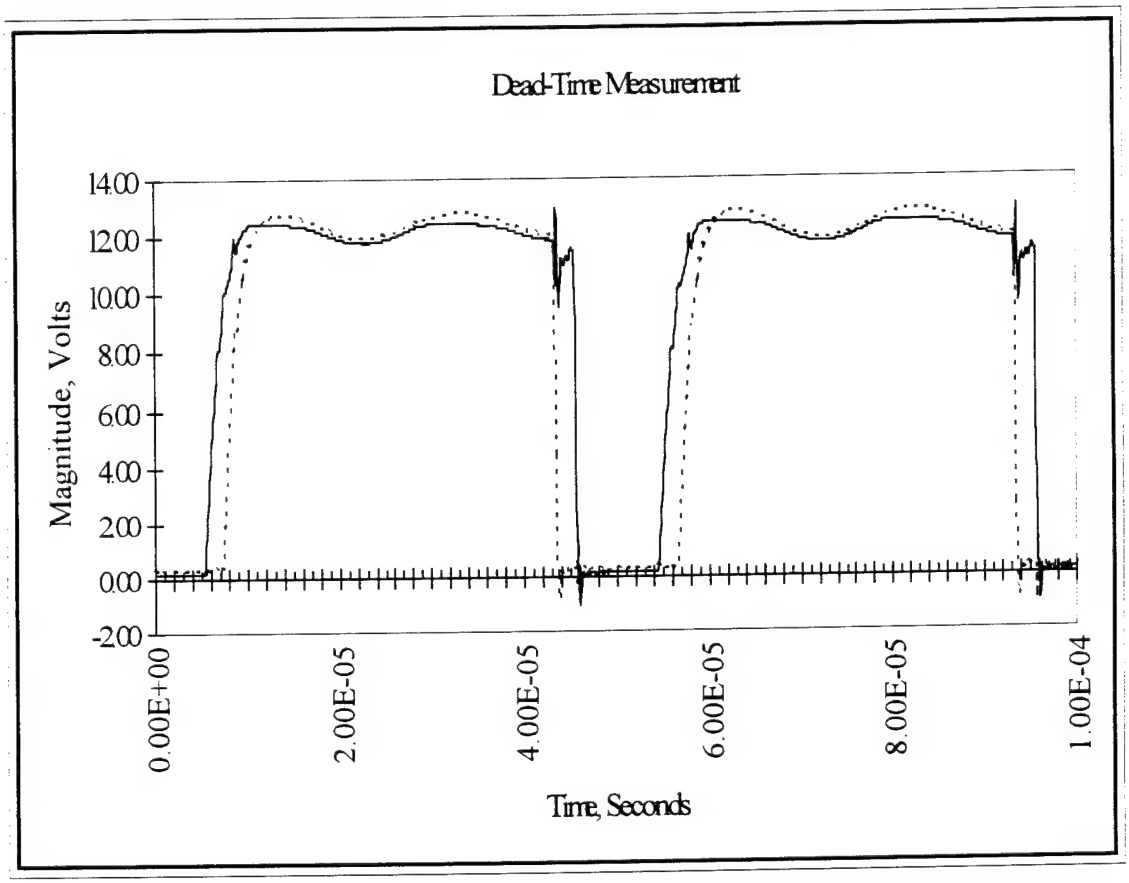

Figure 5.2 Dead-Time Measurement

was measured as approximately 3μSec. At the falling edge the dead-time was measured as 3μSec. The solid line closes the dead-time to a few nanoseconds at the glitch on the falling edge. This presents a problem. The solid line represents the input to the gate of the p-channel MOSFET Q3. This glitch in the waveform seems to be turning on the p-channel MOSFET while the n-channel MOSFET Q4

is still on. Athough only for a few nanoseconds, this represents a power supply short circuit path to ground. The currents can reach 5 Amperes and the MOSFETs tend to burn up. The circuit was run at maximum dead-time to try to eliminate these occurances.

B. POWER OUTPUT MEASUREMENTS

The power output of the system was measured using an ammeter and a voltmeter. None of the circuits tried, provided the power output needed to satisfy the requirements of the power amplifier to interface with the TAR3 driver. The equation for the power output is

$$P = V_{rms} I_{rms} = I_{rms}^{2} R_L \tag{5.1}$$

where R_L is given as the load resistance, I_{rms} is given as the root mean square current through the load resistor, and V_{rms} is the root mean square voltage across the load resistor. The load resistor in our case was a 8.03Ω power resistor. The maximum voltage across the load resistor was found to be 2Vrms. The current through the load resistor was found to be 0.16 Amperes. The final circuit, shown in Figure 2.4, produced this result. The system power is calculated to be .5W. This result was achieved at a frequency of 100Hz, DC power supply input of 10V, input current of 0.18A, percentage modulation of 40%, and switching frequency of 20kHz. The results were disappointing.

C. EFFICIENCY MEASUREMENTS

The efficiency, E, is a ratio of the input power to the output power. The input power is provided by a DC power supply. The input power is the DC

input voltage multiplied by the DC input current. The output power is a measure of the AC voltage at the load resistor multiplied by the AC current through the load resistor. The efficiency, E, is a percentage. The efficiency measured and calculated for this power amplifier system is given by

$$E = \frac{V_{rms} I_{rms}}{V_{SUPPLY} I_{SUPPLY}} \times 100 . \qquad (5.2)$$

The measured efficiency for this power amplifier was found to be only 18%. This result is based on the parameters from the above section.

D. HARMONIC DISTORTION MEASUREMENTS

Harmonic distortion was measured using a spectrum analyzer. The level of the fundamental frequency was measured and then compared to the second through fifth harmonics. The level on the analyzer is given in decibels. The harmonic distortion is measured in percent. The second through fifth hamonics were totaled and compared with the level of the fundamental. Figure 5.3 shows the spectrum of 0 to 200Hz. The fourth harmonic was left off for clarity. The values of the fourth harmonic are 80Hz with a level of -41.07dB. The parameters for the measurement were 20Hz audio input signal, 50kHz carrier wave, and 45% modulation. The harmonic distortion in this case is

$$HD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_{FUNDAMENTAL}} . \qquad (5.3)$$

The result of the equation is less than 3% harmonic distortion. The sixth harmonic and above were neglected because they represented less than .1% of the fundamental.

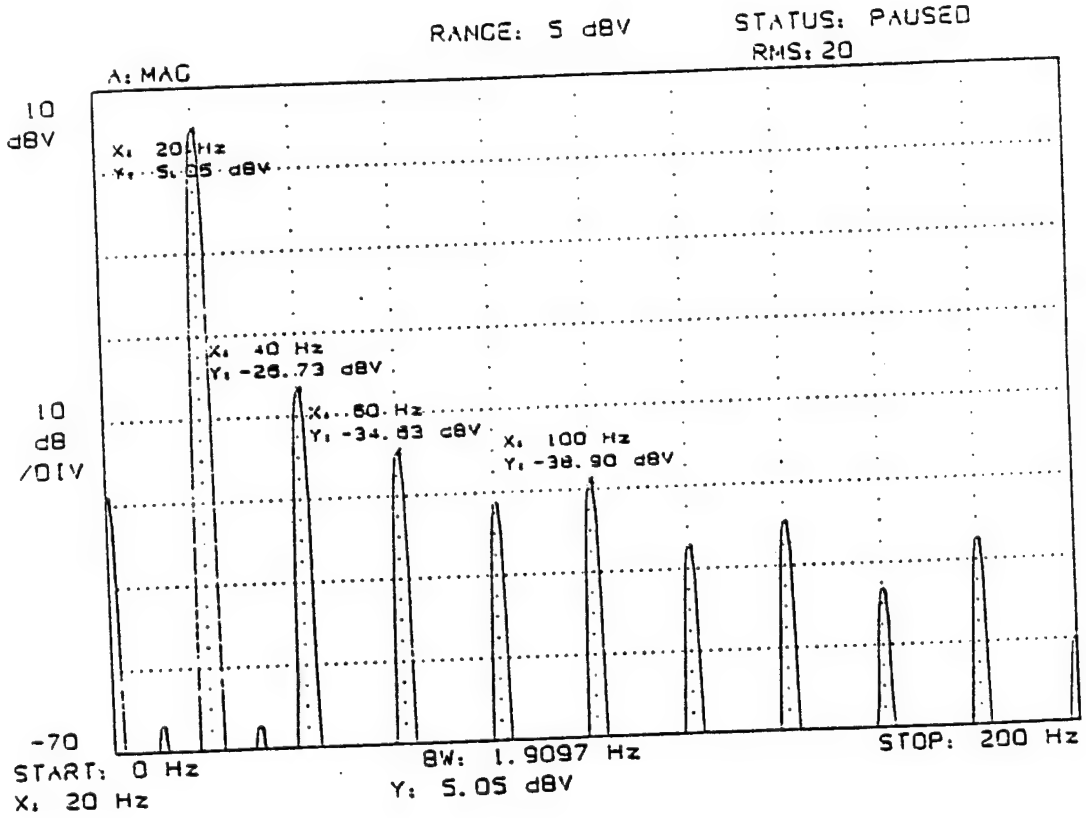

Figure 5.3 Harmonic Distortion Measurement

VI. CONCLUSIONS

The objective of this thesis was to design, build, and test a switching power amplifier for the demonstration thermoacoustic refrigerator (TAR3). The requirements were to design an amplifier that would provide 40 Watts of power with 80% efficiency and 10% harmonic distortion. The harmonic distortion was the only criteria the designed amplifier has satisfied. While the power level for this measurement was low, the modulation level was high. The final circuit resulted in good pulse-width-modulation waveforms and good dead-time generation. The MOSFETs, however, dissipated most of the input power through heat. This occurance can be attributed to power supply shorts to ground due to the n-channel and p-channel MOSFETs simultaneously conducting on the same channel of the bridge. My experience in this thesis has been that switching pulse-width-modulated power amplifiers are extremely difficult to design and build. The theory behind them is relatively simple, but the construction idiosyncrasies were very involved. The recommendations we make are to take great care in avoiding spurious high frequency transients. It may also be true that dead times that are too long may interact with the stray inductances and cause these transients. The gate capacitance of the MOSFETs can be a deciding factor in whether the circuit operates at all. Although this thesis did not provide a workable switching power amplifier for the TAR3 system, the lessons learned in the art of electronics have been invaluable.

APPENDIX

MATLAB PROGRAMS

In this portion of the thesis the two programs written by the author are reproduced verbatim. These programs are B3PFILPG.M and PWM.M. B3PFILPG.M calculates low-pass Butterworth filter parameters for the user given two input values. The program uses the component labels given in Figure 4.3. The program PWM.M models a pulse-width-modulation circuit with four comparators. The triangle frequency is fixed at 20 times the frequency of the input sinusoid. The output of the program displays the modulated output waveforms of the comparators.

```
% B3PFILPG.M
% This Matlab computer program is designed to help an individual
% calculate and plot the frequency response of a 3-Pole Low-Pass
% Butterworth filter. The user is asked to specify two variables
% of the filter. The program then calculates the three remaining
% component values, plots the response, and stores the plot in a
% graphics file name specified by the user.
%

clg
clear

% PROMPT USER FOR PROGRAM HE OR SHE WOULD LIKE TO USE
Q1 = menu('3 Pole Low-Pass Butterworth Filter Calculation Program',...
'User specifies cutoff frequency fc and load resistance RL',...
'User specifies capacitance C and load resistance RL',...
'User specifies Inductance L2 and load resistance RL',...
'User specifies Inductance L1 and load resistance RL','EXIT');
    if Q1 == 1
    filtproa
    elseif Q1 == 2
```

```
filtprob
      elseif Q1 ==3
      filtproc
      elseif Q1 == 4
      filtprod
      elseif Q1 == 5
      break
      end

b3pfilpg
end


% FILTPROA.M
% Given the cutoff frequency fc and the load resistance RL this
% program calculates the inductances and capacitance for a 3rd
% order Low-Pass Butterworth filter.

echo off

% Program start

% Clear all variables and plots stored in memory.

clear
clg

% Prompt user for inputs for the cutoff frequency fc and the load
% resistance RL.

fc=input('Please enter your cutoff frequency, in Hertz: ');
rl=input('Please enter your desired load resistance, in ohms: ');
filename=input('Please enter a plot filename, no extensions, 8 letters max: ','s');

% Calculate the other three components of the filter L1, L2 and C.

l2=rl/(4*pi*fc);
c=2/(3*pi*rl*fc);
l1=1/(2*c*fc^2*pi^2);

% Print the computed values of L1, L2, and C to the screen.
```

```
fprintf('\n\nThe value of L1= %1.9f',l1);
fprintf('\n\nThe value of L2= %1.9f',l2);
fprintf('\n\nThe value for C= %1.9f\n',c);
fprintf('\n\n\nStrike a key for plot....\n');
pause
fprintf('\n\nThe plot will take seconds on a 486 and minutes on a 386\n\n');


% Calculate the frequency response of the transfer function
% for the 3-Pole Low-Pass Butterworth Filter.

format short e
xx=1:1000:100001;
for f=1:1000:100001;
t(f)=rl/(rl+(j*2*pi*f*(l1+l2))-(2*pi*f*2*pi*f*rl*c*l1)-...
(j*2*pi*f*2*pi*f*2*pi*f*l1*l2*c));
t1(f)=abs(t(f));
t2(f)=20*log10(t1(f));
end

% Plot frequency response of the 3-Pole filter to screen.

semilogx(xx,t1(1:1000:100001));
grid
xlabel('FREQUENCY Hz');
ylabel('MAGNITUDE Vo/Vi');
title('FREQUENCY RESPONSE OF 3-POLE BUTTERWORTH FILTER');
pause

% Plot frequency response of the 3-Pole filter to screen,
% Y-axis magnitude now in decibels.

semilogx(xx,t2(1:1000:100001));
grid
xlabel('FREQUENCY in Hz');
ylabel('MAGNITUDE in dB');
title('FREQUENCY RESPONSE OF 3-POLE BUTTERWORTH FILTER');
text(5,-8,'GIVEN:');
text(5,-10,['Load Resistance RL=  ',num2str(rl),' ohms']);
text(5,-13,['Cutoff Frequency fc= ',num2str(fc),' Hertz']);
text(5,-18,'CALCULATED:');
text(5,-20,['Inductor L1= ',num2str(l1),' Henries']);
```

```
text(5,-23,['Inductor L2= ',num2str(l2),' Henries']);
text(5,-26,['Capacitor C= ',num2str(c),' Farads']);
pause

% Store graphics information for printing in file bwfilter.met
meta filename

% Break back to main Program.

end


% FILTPROB.M
% Given the capacitance C and the load resistance RL this
% program calculates the inductances and cutoff frequency
% for a 3rd order Low-Pass Butterworth filter.

echo off

% Program start

% Clear all variables and plots stored in memory.

clear
clg

% Prompt user for inputs for the capacitance C and the load
% resistance RL.

c=input('Please enter your desired capacitance, in FARADS: ');
rl=input('Please enter your desired load resistance, in OHMS: ');

% Calculate the other three components of the filter L1, L2 and fc.

fc=2/(3*pi*rl*c);
l2=rl/(4*pi*fc);
l1=rl/(8*(fc^3)*(pi^3)*l2*c);

% Print the computed values of L1, L2, and C to the screen.

fprintf('\n\nThe value of L1= %1.9f',l1);
fprintf('\n\nThe value of L2= %1.9f',l2);
```

```
fprintf('\n\nThe value for fc= %1.9f\n',fc);
fprintf('\n\n\nStrike a key for plot....\n');
pause
fprintf('\n\nThe plot will take seconds on a 486 and minutes on a 386\n\n');


% Calculate the frequency response of the transfer function
% for the 3-Pole Low-Pass Butterworth Filter.

format short e
xx=1:1000:100001;
for f=1:1000:100001;
t(f)=rl/(rl+(j*2*pi*f*(l1+l2))-(2*pi*f*2*pi*f*rl*c*l1)-(j*2*pi*f*2*pi*f*2*pi*f*l1*l2*c));
t1(f)=abs(t(f));
t2(f)=20*log10(t1(f));
end

% Plot frequency response of the 3-Pole filter to screen.

semilogx(xx,t1(1:1000:100001));
grid
xlabel('FREQUENCY Hz');
ylabel('MAGNITUDE Vo/Vi');
title('FREQUENCY RESPONSE OF 3-POLE BUTTERWORTH FILTER');
pause

% Plot frequency response of the 3-Pole filter to screen,
% Y-axis magnitude now in decibels.

semilogx(xx,t2(1:1000:100001));
grid
xlabel('FREQUENCY in Hz');
ylabel('MAGNITUDE in dB');
title('FREQUENCY RESPONSE OF 3-POLE BUTTERWORTH FILTER');
text(5,-8,'GIVEN:');
text(5,-10,['Load Resistance RL=  ',num2str(rl),' ohms']);
text(5,-13,['Capacitor C= ',num2str(c),' Farads']);
text(5,-18,'CALCULATED:');
text(5,-20,['Inductor L1= ',num2str(l1),' Henries']);
text(5,-23,['Inductor L2= ',num2str(l2),' Henries']);
text(5,-26,['Cutoff Frequency= ',num2str(fc),' Hertz']);
pause
```

```
% Store graphics information for printing in file bwfilter.met
meta bwfilter

% Break back to main Program.

end


% FILTPROC.M
% Given the inductance of L2 and the load resistance RL this
% program calculates the inductance L1, capacitance C, and
% cutoff frequency fc for a 3rd order Low-Pass Butterworth filter.

echo off

% Program start

% Clear all variables and plots stored in memory.

clear
clg

% Prompt user for inputs for inductance L2 and the load
% resistance RL.

l2=input('Please enter the inductance value for L2, in Henries: ');
rl=input('Please enter your desired load resistance, in Ohms: ');

% Calculate the other three components of the filter L1, fc and C.

fc=rl/(4*pi*l2);
c=2/(3*pi*rl*fc);
l1=1/(2*c*fc^2*pi^2);

% Print the computed values of L1, L2, and C to the screen.

fprintf('\n\nThe value of L1= %1.9f',l1);
fprintf('\n\nThe value of fc= %1.9f',fc);
fprintf('\n\nThe value for C= %1.9f\n',c);
fprintf('\n\n\nStrike a key for plot....\n');
pause
```

```
fprintf('\n\nThe plot will take seconds on a 486 and minutes on a 386\n\n');


% Calculate the frequency response of the transfer function
% for the 3-Pole Low-Pass Butterworth Filter.

format short e
xx=1:1000:100001;
for f=1:1000:100001;
t(f)=rl/(rl+(j*2*pi*f*(l1+l2))-(2*pi*f*2*pi*f*rl*c*l1)-(j*2*pi*f*2*pi*f*2*pi*f*l1*l2*c));
t1(f)=abs(t(f));
t2(f)=20*log10(t1(f));
end

% Plot frequency response of the 3-Pole filter to screen.

semilogx(xx,t1(1:1000:100001));
grid
xlabel('FREQUENCY Hz');
ylabel('MAGNITUDE Vo/Vi');
title('FREQUENCY RESPONSE OF 3-POLE BUTTERWORTH FILTER');
pause

% Plot frequency response of the 3-Pole filter to screen,
% Y-axis magnitude now in decibels.

semilogx(xx,t2(1:1000:100001));
grid
xlabel('FREQUENCY in Hz');
ylabel('MAGNITUDE in dB');
title('FREQUENCY RESPONSE OF 3-POLE BUTTERWORTH FILTER');
text(5,-8,'GIVEN:');
text(5,-10,['Load Resistance RL=  ',num2str(rl),' ohms']);
text(5,-13,['Inductor L2= ',num2str(l2),' Henries']);
text(5,-18,'CALCULATED:');
text(5,-20,['Inductor L1= ',num2str(l1),' Henries']);
text(5,-23,['Capacitor C= ',num2str(c),' Farads']);
text(5,-26,['Cutoff Frequency= ',num2str(fc),' Hertz']);
pause

% Store graphics information for printing in file bwfilter.met
meta bwfilter
```

```
% Break back to main Program.

end

% FILTPROD.M
% Given the inductance of L1 and the load resistance RL this
% program calculates the inductance L2, capacitance C, and
% cutoff frequency fc for a 3rd order Low-Pass Butterworth filter.


echo off

% Program start

% Clear all variables and plots stored in memory.

clear
clg

% Prompt user for inputs for inductance L1 and the load
% resistance RL.

l1=input('Please enter the inductance value for L1, in Henries: ');
rl=input('Please enter your desired load resistance, in Ohms: ');

% Calculate the other three components of the filter L2, fc and C.

fc=3*rl/(4*pi*l1);
l2=rl/(4*fc*pi);
c=(l1+l2)/(8*pi^2*l1*l2*fc^2);

% Print the computed values of L1, L2, and C to the screen.

fprintf('\n\nThe value of L2= %1.9f',l2);
fprintf('\n\nThe value of fc= %1.9f',fc);
fprintf('\n\nThe value for C= %1.9f\n',c);
fprintf('\n\n\nStrike a key for plot....\n');
pause
fprintf('\n\nThe plot will take seconds on a 486 and minutes on a 386\n\n');
```

```
% Calculate the frequency response of the transfer function
% for the 3-Pole Low-Pass Butterworth Filter.

format short e
xx=1:1000:100001;
for f=1:1000:100001;
t(f)=rl/(rl+(j*2*pi*f*(l1+l2))-(2*pi*f*2*pi*f*rl*c*l1)-(j*2*pi*f*2*pi*f*2*pi*f*l1*l2*c));
t1(f)=abs(t(f));
t2(f)=20*log10(t1(f));
end

% Plot frequency response of the 3-Pole filter to screen.

semilogx(xx,t1(1:1000:100001));
grid
xlabel('FREQUENCY Hz');
ylabel('MAGNITUDE Vo/Vi');
title('FREQUENCY RESPONSE OF 3-POLE BUTTERWORTH FILTER');
pause

% Plot frequency response of the 3-Pole filter to screen,
% Y-axis magnitude now in decibels.

semilogx(xx,t2(1:1000:100001));
grid
xlabel('FREQUENCY in Hz');
ylabel('MAGNITUDE in dB');
title('FREQUENCY RESPONSE OF 3-POLE BUTTERWORTH FILTER');
text(5,-8,'GIVEN:');
text(5,-10,['Load Resistance RL=  ',num2str(rl),' ohms']);
text(5,-13,['Inductor L1= ',num2str(l1),' Henries']);
text(5,-18,'CALCULATED:');
text(5,-20,['Inductor L2= ',num2str(l2),' Henries']);
text(5,-23,['Capacitor C= ',num2str(c),' Farads']);
text(5,-26,['Cutoff Frequency= ',num2str(fc),' Hertz']);
pause

% Store graphics information for printing in file bwfilter.met
meta bwfilter

% Break back to main Program.
```

```
end


% PWM.M
% Program to Demonstrate Pulse-Width-Modulation for a 25kHz
% triangle wave as the carrier and a 500Hz sine wave as the
% modulating audio signal.

% Eric W. Moore
% August 20, 1993;

% Clear all variables and graphs
clear
clg

% Generate the triangle waveform
x1=triang(49);
x1=[0;x1];

x1=[x1;x1;x1;x1;x1;x1;x1;x1;x1;x1;x1;x1;x1;x1;x1;x1;x1;x1;x1;x1;0];

% Offset the triangle waveforms
x3=1.5+5.*x1;
x1=1+5.*x1;
nplot=0:1000;

%
    for n=1:1001;
        y1(n)=3.5+1.5.*sin(((n-1)*2*pi)/1001);
    end
x2=x1';
pwm1=x2>y1;
axis([0 1000 0 7]);
plot(nplot,x1,'--',nplot,y1,'-');
    title('Triangle Carrier and Audio Signal inputs to U1A');
    xlabel('Time');
    ylabel('Magnitude, Volts');
    text(50,6.7,'Dashed line non-inverting input pin#3 of U1A');
    text(50,6.5,'Solid line input inverting input pin#2 of U1A');
pause
meta tpwm25
```

```
    for n1=1:1001;
        if pwm1(n1)==1
            pw1(n1)=12;
        else
            pw1(n1)=0;
        end
    end

axis([0 1000 -1 13]);
plot(nplot,pw1)
    title('Pulse-Width-Modulation Comparator Output for U1A, no Offset');
    xlabel('Time');
    ylabel('Magnitude, Volts');
    text(50,12.3,'Solid line output of U1A for gate of n-channel FET Q4');

pause
meta tpwm25


x4=x3';
pwm2=x4>y1;
    for n1=1:1001;
        if pwm2(n1)==1
            pw2(n1)=12;
        else
            pw2(n1)=0;
        end
    end

axis([0 1000 0 7]);
plot(nplot,x3,'--',nplot,y1,'-');
    title('Triangle Carrier and Audio Signal inputs to U2A');
    xlabel('Time');
    ylabel('Magnitude, Volts');
    text(50,1.2,'Dashed line non-inverting input pin#3 of U2A');
    text(50,1,'Solid line input inverting input pin#2 of U2A');
    text(50,.8,'Note the offset of the dashed line input for U2A ');
    text(50,.6,'compared to U1A the triangle waveform is now shifted ');
    text(50,.4,'up by .5VDC and goes from 1.5 to 6.5VDC');
pause
meta tpwm25
```

```
axis([0 1000 -1 13]);
plot(nplot,pw2)
     title('Pulse-Width-Modulation Comparator Outputs for U2A, with .5VDC
Offset');
     xlabel('Time');
     ylabel('Magnitude, Volts');
     text(50,12.5,'Output of U2A pin #1 to gate of p-channel FET Q3')

pause
meta tpwm25

axis([0 1000 -1 13]);
plot(nplot,pw1,'-',nplot,pw2,'--');
     title('Pulse-Width-Modulation Comparator Outputs for U1A and U2A');
     xlabel('Time');
     ylabel('Magnitude, Volts');
     text(50,12.5,'Dashed line output of U2A to gate of p-channel FET Q3')
     text(50,-.5,'Solid line output of U1A to gate of n-channel FET Q4')

pause
meta tpwm25

pwm3=y1>x2;
axis([0 1000 0 7]);
for  n1=1:1001;
          if pwm3(n1)==1
               pw3(n1)=12;
          else
               pw3(n1)=0;
          end
     end

axis([0 1000 -1 13]);
plot(nplot,pw3)
     title('Pulse-Width-Modulation Comparator Output for U1B, no Offset');
     xlabel('Time');
     ylabel('Magnitude, Volts');
     text(50,12.3,'Solid line output of U1B for gate of p-channel FET Q1');

pause
meta tpwm25
```

```
x4=x3';
pwm4=y1>x4;
    for n1=1:1001;
        if pwm4(n1)==1
            pw4(n1)=12;
        else
            pw4(n1)=0;
        end
    end

axis([0 1000 -1 13]);
plot(nplot,pw4)
    title('Pulse-Width-Modulation Comparator Outputs for U2B, with .5VDC
Offset');
    xlabel('Time');
    ylabel('Magnitude, Volts');
    text(50,12.5,'Output of U2B pin #7 to gate of n-channel FET Q2')

pause
meta tpwm25

axis([0 1000 -1 13]);
plot(nplot,pw3,'--',nplot,pw4,'-');
    title('Pulse-Width-Modulation Comparator Outputs for U1B and U2B');
    xlabel('Time');
    ylabel('Magnitude, Volts');
    text(50,12.5,'Dashed line output of U1B to gate of p-channel FET Q1')
    text(50,-.5,'Solid line output of U2B to gate of n-channel FET Q2')

pause
meta tpwm25

plot(nplot,pw3,'--',nplot,pw1,'-');
    title('Pulse-Width-Modulation Comparator Outputs for U1A and U1B');
    xlabel('Time');
    ylabel('Magnitude, Volts');
    text(50,12.5,'Dashed line output of U1B to gate of p-channel FET Q1')
    text(50,-.5,'Solid line output of U1A to gate of n-channel FET Q4')

pause
meta tpwm25
```

```
plot(nplot,pw2,'--',nplot,pw4,'-');
    title('Pulse-Width-Modulation Comparator Outputs for U2A and U2B');
    xlabel('Time');
    ylabel('Magnitude, Volts');
    text(50,12.5,'Dashed line output of U1A to gate of p-channel FET Q3')
    text(50,-.5,'Solid line output of U2B to gate of n-channel FET Q2')


end
```

REFERENCES

1. Decker, L., *Class S Power Amplifier*, Linear Products Showcase, p. 10, Fall/Winter, Texas Instruments Press, Dallas, Texas, 1991.

2. Rott, A. N., *Thermoacoustics*, Adv. Appl. Mech. 20, 135 (1980).

3. Hofler, T. J., "Thermoacoustic Refrigeration Design and Performance", Ph.D. Dissertation, University of California, San Diego, California, 1986.

4. Oppenheim, A. V., Willsky, A. S., and Young, I. T., *Signals and Systems*, Prentice-Hall, Englewood Cliffs, New Jersey, 1983.

5. Texas Instruments Staff, *Linear Circuits, Voltage References and Supervisors Data Book* Vol. 3, Texas Instruments Press, Dallas, Texas, 1989.

INITIAL DISTRIBUTION LIST

1.	Defense Technical Information Center Cameron Station Alexandria, Virginia 22304-6145	2
2.	Library, Code 52 Naval Postgraduate School Monterey, California 93943-5101	2
3.	Chairman, Code EC Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5121	1
4.	Professor Sherif Michael, Code EC/Mi Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5121	1
5.	Professor T. J. Hofler, Code PH/Hf Department of Physics Naval Postgraduate School Monterey, California 93943-5117	2
6.	Mr. E. W. Moore 1101 Spruce St. Hinesville, Georgia 31313	2